Curriculum Vitae et Studiorum

Graziano Pravadelli

1. Personal data

Place and date of birth:

- Legnago (VR) Italy, 04 July 1974.

Marital status:

- Married since July 2003, two sons.

Current positions:

- Full professor, Università degli Studi di Verona, Italy, since October 2018;
- President of quality assurance board (Presidio della Qualità), Università degli Studi di Verona, Italy, since July 2017;
- Member of the Albo "Esperti della Valutazione – Profilo Esperti Disciplinari" and collaborator of the Italian National Agency for the Evaluation of Universities and Research Institute (ANVUR) for the 09 Area, since July 2015.
- Co-founder and co-owner of EDALab s.r.l. (http://www.edalab.it), since July 2007.

Previous positions:

- Associate professor, Università degli Studi di Verona, Italy, from January 2011 to September 2018;
- Assistant professor, Università degli Studi di Verona, Italy, from January 2005 to December 2010;
- Post-doc, Università degli Studi di Verona, Italy, from April 2004 to December 2004.

Scientific memberships:

- IEEE senior member.

Working address and contacts:

- Dipartimento di Informatica, Università degli Studi di Verona.
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2. National scientific qualifications

- National Scientific Qualification for full professor (01/B1) acquired on 19/01/2015.
- National Scientific Qualification for full professor (09/H1) acquired on 04/04/2017.

3. Higher education

Ph.D.:

- Ph.D., Computer Science, Università degli Studi di Verona, Italy, March 2004. Thesis title: "*Using functional verification to evaluate the accuracy of model checking applied to embedded systems: theory and application*" (advisor: Prof. Franco Fummi).

Laurea:

- Laurea degree (summa cum laude), Computer Science, Università degli Studi di Verona, Italy, April 2001. Thesis title (in Italian): "*Simulazione di errore per descrizioni VHDL e SystemC per il test funzionale*" ("*Functional test by fault simulation for VHLD and SystemC models*") (advisor: Prof. Franco Fummi).

4. Awards

Best paper candidate:

- Danese, F. Filini, G. Pravadelli, *"A Time-Window Based Approach for Dynamic Assertions Mining on Control Signals"*. In: IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC). Daejeon, Korea, 5-7 October 2015.
- F. Cucchetto, A. Lonardi, G. Pravadelli, *"A common architecture for co-simulation of SystemC models in QEMU and OVP virtual platforms"*. In: FIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC). Playa del Carmen, Mexico, 6-8 October 2014.
- M. Bonato, G. Di Guglielmo, M. Fujita, F. Fummi, G. Pravadelli, *"Dynamic property mining for embedded software"*. In: ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS). Tampere, Finland, 7-12 October 2012.
- N. Bombieri, F. Fummi, G. Pravadelli, *"A Mutation Model for the SystemC TLM 2.0 Communication Interfaces"*. In: ACM/IEEE Design, Automation and Test in Europe (DATE). Munich, Germany, 10-14 March 2008.

Selected best paper:

- G. Di Guglielmo, F. Fummi, C. Marconcini, G. Pravadelli, *"FATE: a Functional ATPG to Traverse unstabilized EFSMs"*. In: IEEE European Test Symposium (ETS). Southampton, UK, 21-24 May 2006.

Technology transfer:

- Special mention *"Best National Social Innovation Project"* at Premio Nazionale per l'Innovazione 2017 (National Prize for Innovation) with the project *"ADA - Assisting Daily life Activities, an ICT-based virtual coaching system to support elderly in activities of daily life"*, 1 December 2017.

5. Research interests

Graziano Pravadelli is member of the research group in Electronic System Design (ESD) at the Department of Computer Science of the Università degli Studi di Verona, Italy. The research interests of Graziano Pravadelli concern the main aspects of system-level design of embedded systems. In particular, his activity is related to the following main fields, partially supported by the research projects reported in Section 6:

1. Modelling and simulation of embedded systems;
2. Semi-formal approaches for embedded system verification;
3. Fault models and test generation for embedded systems;
4. Embedded systems for virtual coaching of daily life activities.

In this context, he has cooperated with several international institutions like, for example, University of Paderbon (Germany), University of Tokyo (Japan), University of Michigan (USA), University of Southampton (UK), University of California at Irvine (USA), Tallinn University of Technology (Estonia), Linkoeping University (Sweden), University of Graz (Austria), University of Cantabria (Spain), OFFIS (Germany), FBK (Italy), CEA-LETI (France), STMicroelectronics (Italy), Agilent – now Keysight Technologies (UK), SpringSoft – acquired by Synopsys (France).

5.1 Modelling and simulation of embedded systems

The ever increasing complexity of modern embedded systems requires that designers consider heterogeneous and often conflicting aspects, such as, for example, the adoption of different levels of abstraction, the integration of digital and analog components, the use of HW-dependent software, the awareness of the presence of a physical environment in which the system is embedded, etc. This heterogeneity has been addressed through various modelling and simulation approaches, by adopting both top-down and bottom-up methodologies, and by integrating model-based design, component-based design and co-simulation-based techniques. However, it is evident the lack of a computational model widely accepted that allows integrating heterogeneous components in a homogeneous description that can be easily manipulated and simulated during the various stages of the design flow.

In this context, Graziano Pravadelli coordinated the definition and implementation of a virtual prototyping and modelling environment for embedded systems (HIFSuite – http://www.hifsuite.com) based on the HIF (Heterogeneous Intermediate Format) interchange format, and the definition of the UNIVERcm (Universal Versatile Computational Model) computational model that allows to formalize the semantics of HIF descriptions. Based on HIFSuite, Graziano Pravadelli eventually set up various techniques and methodologies for modelling, integration, simulation and verification of embedded systems. Of particular interest it is the definition of an automatic technique for the abstraction of RTL (Register Transfer Level) models to TLM (Transaction Level Model) models, which avoids the co-

simulation of mixed-RTL-TLM descriptions that slows down the simulation speed, to take full advantage of the greater speed of TLM models.

Recently, Graziano Pravadelli has moved his attention also towards system-level modeling of extra-functional properties, targeting, in particular, power behaviors of digital IPs. In this field he proposed an innovative approach for the automatic generation of power state machines (PSMs) that allow validating the power consumption of a system inside a virtual prototype. Currently, none other approach exists in the literature that automatically generate PSMs. The approach starts by dynamically mining temporal assertions from the functional traces. From them, the states and the transitions of a corresponding set of PSMs are generated and optimized by exploiting a calibration process relying on a set of training power traces. Future research activities in this context will be devoted to address the generation of PSMs for time-dependent and data dependent designs and their abstraction towards the TLM level.

Most of the activities related to HIFSuite and UNIVERcm were made as part of European projects SYMBAD, VERTIGO, CONTREX, COMPLEX, SMAC and TOUCHMORE for which HIFSuite has become the main tool for the creation of virtual platforms for simulation and verification of complex systems. HIFSuite is currently a commercial product of EDALab.

5.2 Semi-formal approaches for embedded system verification

In the context of verification of embedded systems, the research activities of Graziano Pravadelli focuses on the definition of semi-formal techniques and, in particular, on the study of approaches for automation and optimization of verification methodologies based on assertions. In this context, the main covered research fields are:

- Assertion-based verification for embedded software. The main contribution of Graziano Pravadelli is represented by having defined a methodology and an automated tool (radCHECK - http://www.verificationsuite.com) to apply assertion-based verification (ABV) to the world of embedded SW. ABV techniques are mainly oriented to check descriptions based on transition systems (e.g., extended finite state machines) typical of the RTL abstraction level, where the time reference for synchronization of models and checkers (simulated components corresponding to the desired assertions) is closely related to the concept of clock cycle. In the context of the embedded software, the absence of such a precise time reference makes it much more difficult to apply ABV techniques. This limitation has been overcome by Graziano Pravadelli's research activity through the principles of model-based modelling. The research has led the implementation of radCHECK, an automated tool for assertion-based verification of embedded software developed under the VAFER project. radCHECK has been marketed by STMProducts and developed in collaboration with EDALab with the scientific supervision of Graziano Pravadelli. Other relevant contributions were produced as part of the optimization of assertions in real-time systems, to avoid that the timing constraints imposed by such systems

were missed because of the time required for the verification of statements in a context of self-checking.

- Automatic generation of assertions. In these works, the traditional flow that involves first defining assertions corresponding to the specifications and then checking them has been reversed. Graziano Pravadelli has proposed methods for automatic extraction of temporal assertions from simulation traces of HW/SW descriptions. Mined assertions can then be compared with the initial specifications to analyze the presence of discrepancies, which would be symptom of an incorrect implementation. Compared to techniques already existing in the literature that extract only Boolean properties, the approaches proposed by Graziano Pravadelli are distinguished by the ability to generate assertions that predicate both at Boolean and non-Boolean domains by extracting arithmetic-logic expression on Boolean, integer and float data types. Extraction of invariants, i.e., arithmetic logic expressions that represent a stable condition holding on the analyzed execution traces, has been investigated too by proposing efficient strategies exploiting the power of GPU architecture for speeding-up the mining phase.
- Reuse and automatic abstraction of assertions. The issues related to the integration and simulation of descriptions represented at different levels of abstraction (e.g., RLT and TLM) and on different domains (e.g., analog, digital) have a great impact in the context of verification too. An assertion initially written for an analog model cannot be reused to check the corresponding digital model after its discretization. Similarly, an assertion defined at RTL level need to be rewritten when moving towards the TLM level. In this context, the activity of Graziano Pravadelli was concentrated in the definition of methodologies for the automatic reuse and abstraction of assertions between different domains and abstraction levels in order to avoid costly (in terms of time) and risky (in terms of errors that can be introduced) manuals redefinition. In particular, while there are several works that propose approaches for re-use of assertions from TLM to RTL, the abstraction of assertions from RTL to TLM has been addressed for the first time by Graziano Pravadelli.
- Assertion qualification. The lack of exhaustiveness is one of the biggest problems related to the use of simulation-based techniques for digital system validation. Formal verification aims at overcoming this problem by proving assertions on mathematical models representing the system implementation. In this context, temporal logic assertions are defined to formally check the correctness of a design implementation with respect to the specification. However, the use of assertions cannot completely assure the correctness of the design implementation. Assertion's vacuity, incompleteness and inconsistency may prevent the effectiveness of assertion-based verification approaches, leading the verification engineers to a false sense of security. To improve the degree of confidence on assertion-based verification, Graziano Pravadelli has proposed several techniques to qualify the set of assertions in terms of design coverage, vacuity analysis, and degree of interestingness, when used for checking the correctness of a model. The work of Graziano Pravadelli distinguishes from previous approaches since it is based on mutant

analysis rather than symbolic methods, which guarantees a more accurate estimation of assertion quality in a shorter time.

- Assertion based verification for hardware security. In the past decade, globalization of hardware design and fabrication processes have raised serious concerns about hardware-based attacks. In addition, the number of firmware attacks have been on the rise. Thus, more sophisticated validation techniques and tools are necessary to guarantee an effective identification of hardware and firmware vulnerabilities. In this field, Graziano Pravadelli has defined a verification approach that detects different types of hardware trojans in RTL models by exploiting an efficient control-flow subgraph matching algorithm. Moreover, he has developed a tool that automatically generates formal assertions to identify the unlikely execution flows of a firmware, where security vulnerabilities can escape generic validation efforts.

Part of the activities related to the semi-formal-verification of embedded systems have been undertaken under the projects EFFORT, VAFER, OPTIMUM and SMAC.

5.3 Fault models and test generation for embedded systems

Automatic test pattern generation is the basis of all the verification techniques that are based on simulation. Very often this generation is driven by metrics that require the application of fault models to simulate the presence of errors (design) or defects (physical) within the model and/or its implementation. Such metrics measure the quality of the generated sequences according to their ability to "find" faults injected by comparing the results of the fault-free model/implementation with those of the models/implementations perturbed by faults. In this context, Graziano Pravadelli has proposed numerous techniques for the generation of test sequences integrating symbolic, concolic and concrete approaches. In addition, Graziano Pravadelli defined a language for specifying test sequences (Testbench Specification Language) particularly suitable to represent constraints that must be met to activate (and then test) special conditions that would not be analyzed by using traditional probabilistic approaches and that would require too space-time consuming resources for an exhaustive evaluation.

Graziano Pravadelli worked also on fault modelling strategies, both for hardware descriptions and embedded software. In particular, it is worth noting that Graziano Pravadelli proposed for the first time a fault model for TLM descriptions.

Most of the activities related to the semi-formal-verification of embedded systems were carried on as part of the VAFER and OPTIMUM projects.

5.4 Embedded systems for virtual coaching of daily life activities

Since 2017, Graziano Pravadelli has started a new multidisciplinary research activity for the definition of virtual coaching systems to assists people with special needs in daily life activities. In this context, he is working on the definition of a virtual coaching architecture, based on the integration among smart objects, wearable devices and intelligent algorithms to automatically recognize people needs and provide

them support in the accomplishment of daily life activities. In particular, Graziano Pravadelli is focusing the coaching system towards elderly and persons with physical or cognitive impairments. First results of this research activities are the definition of a low-cost mechanism for indoor localization of coachees, and the definition of an algorithm to recognize freezing of gait in people affected by Parkinson's disease.

Most of the activities related to the use of embedded systems for virtual coaching are carried on as part of the FOLLOWME, ADA and BIPBIP projects, which involve the cooperation between computer scientists, medical doctors and psychologists.

6. Coordination of and participation to research activities

Graziano Pravadelli has participated to the activities of several national and international research projects as reported in the following sections.

6.1 Participation to funded European projects with peer review

1. Title: Design of embedded mixed-criticality control systems under consideration of extra-functional properties (CONTREX FP7-ICT-2013-10-611146)
   Funding organization: European commission
   Funding schema: Large-scale integrating project
   Period: October 2013 – September 2016
   Number of participants: 15
   Achieved contribution: € 241520
   Role in the project: project leader of "system analysis, validation and exploration" of EDALab research unit and project manager of HIFSuite development.
2. Title: Smart system co-design (SMAC FP7-ICT-2011-7-288827)
   Funding organization: European commission
   Funding schema: Large-scale integrating project
   Period: October 2011 – March 2015
   Number of participants: 17
   Achieved contribution: € 473096
   Role in the project: project leader of work package 2 concerning the "co-simulation platform" for EDALab research unit and project manager of HIFSuite development.
3. Title: Automatic Customizable Tool-chain for Heterogeneous Multicore Platform Software Development (TOUCHMORE FP7-ICT-2011-7-288166)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: September 2011 – September 2014
   Number of participants: 8
   Achieved contribution: € 300000
   Role in the project: project manager of HIFSuite development.

4. Title: Codesign and power management in platform-based design space exploration (COMPLEX FP7-ICT-4-247999)
   Funding organization: European commission
   Funding schema: Large-scale integrating project
   Period: December 2009 – November 2012
   Number of participants: 15
   Achieved contribution: € 240000
   Role in the project: project manager of HIFSuite development.
5. Title: A correct by construction workbench for design and verification of embedded systems (COCONUT FP7-2007-IST-1-217069)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: January 2008 - June 2010
   Number of participants: 10
   Achieved contribution: € 340000
   Role in the project: discrete system project manager.
6. Title: Verification and validation of embedded design workbench (VERTIGO IST-2006-033709)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: June 2006 - November 2008
   Number of participants: 7
   Achieved contribution: € 346000
   Role in the project: technical responsible of the research unit.
7. Title: Formal verification in system level based design (SYMBAD IST-2001-34607)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: March 2002 - October 2004
   Number of participants: 4
   Achieved contribution: € 290000
   Role in the project: coordinator of the development of the research unit applications.

6.2 Coordination of funded national projects with peer review

1. Title: BIPBIP: a wearable smart system to prevent freezing of gait in people affected by Parkinson's disease
   Funding organization: Veneto Region
   Funding schema: La ricerca a sostegno della trasformazione aziendale - Innovatori in azienda – assegni di ricerca 2018
   Period: October 2018 – September 2019

Number of participants: 3
Achieved contribution: € 74500
Role in the project: coordinator.

2. Title: ADA: An IoT-based virtual coaching platform for assisting daily life activities of ageing persons with Down syndrome
   Funding organization: Piccola Fraternità Onlus (Verona), Università degli Studi di Verona
   Funding schema: Joint project 2017, Università degli Studi di Verona
   Period: December 2017 – November 2019
   Number of participants: 2
   Achieved contribution: € 36200
   Role in the project: coordinator.
3. Title: FOLLOWME: an interactive platform to support guided tours in telepresence
   Funding organization: Veneto region
   Funding schema: Assegni di ricerca – Sviluppo del potenziale umano nella ricerca e nell'innovazione per una crescita intelligente
   Period: September 2016 – October 2017
   Number of participants: 3
   Achieved contribution: € 41950
   Role in the project: coordinator.
4. Title: Smart pole WSN network (SPAWNE)
   Funding organization: Telefin s.p.a (Verona), Università degli Studi di Verona
   Funding schema: Joint project 2014, Università degli Studi di Verona
   Period: January 2015 – December 2015
   Number of participants: 2
   Achieved contribution: € 31220
   Role in the project: coordinator.
5. Title: Formal verification of embedded Systems (VAFER)
   Funding organization: Veneto region.
   Funding schema: Regional project to support industrial research activity, experimental analysis, innovation and technological dissemination (L.R. n.9 18/05/2007)
   Period: October 2010 – September 2012
   Number of participants: 4
   Achieved contribution: € 183000
   Role in the project: coordinator.

6.3 Participation to funded national projects with peer review

1. Title: Manifattura predittiva: progettazione, sviluppo e implementazione di soluzioni di Digital Manufacturing per la previsione della qualità e la manutenzione intelligente (Predictive

manufacturing: design, development and implementation of Digital Manufacturing solutions for the forecasting of quality and maintenance) (PREMANI)
Funding organization: Veneto region
Funding schema: Azione 1.1.4 "Sostegno alle attività collaborative di R&S per lo sviluppo di nuove tecnologie sostenibili, di nuovi prodotti e servizi"
Period: November 2017 – November 2020
Number of participants: 18
Achieved contribution: € 224540
Role in the project: project manager for the tasks related to verification

2. Title: TOward Industrial Smart DisplaYS (TOYS)
   Funding organization: Exor International (Verona), Università degli Studi di Verona
   Funding schema: Joint project 2015 Università degli Studi di Verona
   Period: January 2016 – December 2016
   Number of participants: 2
   Achieved contribution: € 64000
   Role in the project: project manager for the tasks related to verification
3. Title: Optimizing dependability via mutation analysis for microelectronics (OPTIMUM)
   Funding organization: STM Products (Verona), Università degli Studi di Verona
   Funding schema: Joint project 2010 Università degli Studi di Verona
   Period: January 2011 – December 2012
   Number of participants: 2
   Achieved contribution: € 85500
   Role in the project: project manager.
4. Title: An EFSM-based Framework for Designing and Verifying Embedded Software (EFFORT)
   Funding organization: STM Products (Verona), Università degli Studi di Verona
   Funding schema: Joint project 2007 Università degli Studi di Verona
   Period: January 2008 – December 2009
   Number of participants: 2
   Achieved contribution: € 142000
   Role in the project: project manager.
5. Title: Yield Improvement in Nanotechnology Production Process of Standard Cells Based Integrated Circuits (ImpNanoIC)
   Funding organization: PDF Solutions (Brescia), Università degli Studi di Verona
   Funding schema: Joint project 2005 Università degli Studi di Verona
   Period: January 2007 – December 2007
   Number of participants: 2
   Achieved contribution: € 51000
   Role in the project: project manager.

6. Title: Modeling, simulation and verification of MPSoC platforms (PRIN05)
   Funding organization: Italian Research Ministry (MIUR)
   Funding schema: National interest research project (PRIN)
   Period: January 2006 – December 2008
   Number of participants: 5
   Achieved contribution: € 41000
   Role in the project: technical manager of the research unit.
7. Title: Modeling, simulation and validation of system on chips (PRIN02)
   Funding organization: Italian Research Ministry (MIUR)
   Funding schema: National interest research project (PRIN)
   Period: May 2002 – April 2004
   Number of participants: 6
   Achieved contribution: € 52000
   Role in the project: Coordinator of the development of research unit applications.
8. Title: Modeling and simulation of complex integrated systems for multimedia applications (CNR01)
   Funding organization: National research center (CNR)
   Funding schema: research project
   Period: October 2001 – September 2002
   Number of participants: 4
   Achieved contribution: € 40000
   Role in the project: Coordinator of the development of research unit applications.

6.4 Coordination of industrial projects

1. Title: Acquisition of new knowledges for a wearable system to identify the direction of electromagnetic waves
   Funding organization: Wagoo Italia s.r.l.s. (Verona)
   Period: August 2017 – July 2018
   Number of participants: 2
   Achieved contribution: € 51000
   Role in the project: coordinator
2. Title: An innovative system for monitoring and control based on wireless sensors
   Funding organization: ABS Computers (Verona)
   Period: January 2012 – December 2012
   Number of participants: 2
   Achieved contribution: € 30000
   Role in the project: coordinator

3. Title: Localization of Visual Studio 2012 MSDN Library
   Funding organization: Microsoft Corp. Redmond USA
   Period: October 2013 – April 2014
   Number of participants: 2
   Achieved contribution: € 10000
   Role in the project: coordinator
4. Title: Localization of Visual Studio 2011 MSDN Library
   Funding organization: Microsoft Corp. Redmond USA
   Period: June 2012 – September 2012
   Number of participants: 2
   Achieved contribution: € 15000
   Role in the project: coordinator

6.5 Participation to industrial projects

1. Title: Development of an automatic system for the validation of a development environment of embedded SW
   Funding organization: STM Products (Verona)
   Funding schema: Industrial project
   Period: April 2009 – December 2009
   Number of participants: 2
   Achieved contribution: € 70000
   Role in the project: project manager.
2. Title: Application of an hybrid methodology for functional verification based on formal techniques and test pattern generation (STM01)
   Funding organization: STMicroelectronics (Agrate Brianza)
   Funding schema: industrial project
   Period: May 2001 – April 2002
   Number of participants: 2
   Achieved contribution: € 25000
   Role in the project: coordinator of the development of applications.

7. Organization of and participation to international conferences

Graziano Pravadelli has taken the following roles in international conferences:

- IEEE/IFIP International conference on VLSI-SOC (VLSI-SOC):
  - General chair in 2018;
  - Track chair of “Prototyping, Verification, Modeling, and Simulation” from 2015 to 2017;
  - Member of the TPC since 2010;

- ACM/IEEE Design, Automation and Test in Europe (DATE):
  - Topic chair of "System simulation and validation" in 2019;
  - Topic co-chair of "System simulation and validation" in 2018;
  - Member of the TPC since 2017;
- Forum on Specification and Design Languages (FDL):
  - Member of the steering committee since 2017;
  - Finance chair in 2018 and 2017;
  - Local arrangement chair in 2017;
  - Trach chair of "Tools and techniques" in 2016;
  - Member of the TPC since 2016;
- ACM/IEEE Design Automation Conference (DAC)
  - Member of the TPC in 2018;
- ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
  - Member of the TPC since 2011;
- ACM/IEEE Network on chip symposium (NOCS)
  - Finance chair in 2014;
- IEEE VLSI Design Conference (VLSID)
  - Member of the TPC since 2018;
- IEEE Biennal Baltic Electronic Conference (BEC)
  - Member of the TPC since 2008;
- International Conference on Information and Software Technologies (ICIST)
  - Member of the TPC from 2014 to 2016;
- Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)
  - Member of the TPC from 2008 to 2012.

Graziano Pravadelli has been organizer and speaker of the following tutorials at international conferences:

- Methods and tools for smart device integration and simulation
  In ACM/IEEE Embedded Systems Week (ESWEEK) 2014, New Delhi, India
- Assertion-based verification: a Common Verification Infrastructure for SoC and Embedded Software.
  In ACM/IEEE Design, Automation and Test in Europe (DATE) 2013, Grenoble, France.
- Assertion-based verification for SoC and embedded software.
  In ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) 2012, Sydney, Australia.

Finally, Graziano Pravadelli presented more than 30 contributions at the following international conferences: ACM/IEEE CODES+ISSS, ACM/IEEE DAC, ACM/IEEE DATE, IEEE ETS, ACM GLSVLSI, IEEE HLDVT, IEEE MEMOCODE, IEEE FDL, IFIP/IEEE VLSI-SOC, IEEE DFT, IEEE LATS, IEEE VTS.

8. Referee activities

Graziano Pravadelli has cooperated as reviewer for:

- several international conferences: ACM/IEEE CODES+ISSS, ACM/IEEE DAC, ACM/IEEE DATE, IEEE ETS, ACM GLSVLSI, IEEE HLDVT, IEEE ITC, IEEE MEMOCODE, IEEE MTV, IEEE BEC, IEEE FDL, IEEE ICCAD, IFIP/IEEE VLSI-SOC, IEEE VLSID;
- several international journals: ACM Transactions on Design Automation of Electronic Systems, ACM Transactions on Embedded Computing, ACM Transactions on Architecture and Code Optimization, IEEE Transaction on Computers, IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Kluwer International Journal of Parallel Programming, Springer Design Automation for Embedded Systems, Springer Journal of Electronic Testing, Elsevier Microprocessors and Microsystems, Eurasip Journal of Embedded Systems, IEEE Electronic Notes, Elsevier Integration, The VLSI Journal, Elsevier Information and Software Technology, Elsevier Journal of Systems and Software.

In addition, Graziano Pravadelli has served as referee for the Italian Ministry of University and Research (MIUR) in the following context:

- evaluation of the research of Italian Universities and Research Centers (VQR 2011-2014);
- evaluation of projects submitted to “Progetti di Ricerca Industriale e Sviluppo Sperimentale nelle 12 Aree di specializzazione individuate dal PNR 2015 – 2020”.

Finally, Graziano Pravadelli has participated as member of 7 commissions for the final graduation of PhD students at the following universities:

- Università degli Studi di Verona, Italy, on May 2016 and May 2018;
- Politecnico di Torino, Italy, on July 2017 and May 2018;
- Politecnico di Milano, Italy, on January 2016;
- Università degli Studi di Ferrara, Italy, on April 2016;
- Tallinn University of Technology, Estonia, on June 2013.

9. Teaching activities

Graziano Pravadelli’s teaching activities include:

- Teaching activities at Università degli Studi di Verona, Italy:
    - Sistemi operativi (Operating systems), Laurea in Informatica: 14 courses from 10/2004 till now, more than 1000 teaching hours as coordinator of the course;

  - Sistemi operativi avanzati (Advanced operating systems), Laurea specialistica in Informatica and Laurea magistrale in ingegneria e scienze informatiche: 14 courses from 10/2004 till now, more than 800 teaching hours as coordinator of the course;
  - Software per sistemi embedded (Design automation of embedded systems), Laurea magistrale in ingegneria e scienze informatiche (9 courses from 10/2009 till now, more than 200 teaching hours, as responsible of 1/3 of the course;
  - Informatica (Informatics), Laurea in Lingue e culture per il turismo e il commercio internazionale and Laurea in Scienze delle Attività Motorie e Sportive : 8 courses from 03/2009 to 02/2014, more than 150 teaching hours as coordinator of the course.
  - Sistemi embedded (Embedded system), TANDEM project for future students, http://tandem.univr.it/: 4 courses from 01/2014 till 04/2018, 80 hours as coordinator of the course.
  - Informatica di base (Basic informatics), TANDEM project for future students, http://tandem.univr.it/: 4 courses from 01/2014 till 04/2018, 80 hours as coordinator of the course.

- Teaching activities at Università degli Studi di Trento, Italy:
  - Sistemi operativi (Operating systems), Laura in Informatica: 2 courses from 02/2015 to 01/2017, 120 of teaching hours as coordinator of the course.
- Teaching activities at Politecnico di Milano, Italy:
  - Informatica B (Informatics B), Laurea in Ingegneria Meccanica: 15 courses from 09/2002 till 01/2017, more than 1100 hours as responsible of exercitation and laboratory.

10. Evaluation of the teaching activities by students

The following table shows the results of the student evaluation of the last three academic years for the courses on which Graziano Pravadelli acted as coordinator or co-teacher, based on the survey system adopted by the university where the teaching activity was carried out.

Academic year	**University**	**Course**	**Number of student evaluations**	**Graziano Pravadelli's course score (max = 4)**	**Average score of the courses belonging to the same degree (max = 4)**
2014-15	Università degli Studi di Trento	Sistemi operativi	100	3.49	3.13
2014-15	Università degli Studi di Verona	Sistemi operativi	75	3.27	3.22

2014-15	Università degli Studi di Verona	Sistemi operativi avanzati	17	3.75	3.23
2014-15	Università degli Studi di Verona	SW per sistemi embedded	14	3.23	3.23
2015-16	Università degli Studi di Trento	Sistemi operativi	94	3.48	3.36
2015-16	Università degli Studi di Verona	Sistemi operativi	97	3.15	3.15
2015-16	Università degli Studi di Verona	Sistemi operativi avanzati	11	3.74	3.22
2015-16	Università degli Studi di Verona	SW per sistemi embedded	13	3.30	3.22
2016-17	Università degli Studi di Verona	Sistemi operativi	114	3.31	3.16
2016-17	Università degli Studi di Verona	Sistemi operativi avanzati	9	3.63	3.30
2016-17	Università degli Studi di Verona	SW per sistemi embedded	10	3.45	3.30

11. Advising activities

Graziano Pravadelli's advising activities include:

- Advising of 3 PhD students at Università degli Studi di Verona, Italy:
    - Tara Ghasempouri, *"Improving ABV by automatic generation and abstraction of PSL assertions"*. Graduation date: May 2016. Current position: Research fellow at Tallinn University of Technology, Estonia.
    - Alessandro Danese, *"System-level functional and extra-functional characterization of SoCs through assertion mining"*. Graduation date: May 2018. Current position: Research fellow at Università degli Studi di Verona, Italy.
    - Florenc Demrozi, "*IoT for ambient assisted living*". Expected graduation date: May 2020.
- Co-advising of 6 PhD students at Università degli Studi di Verona, Italy:
    - Valerio Guarnieri, *"Design and verification techniques for TLM-based design flows"*, Graduation date: May 2013. Current position: Project manager at ASEM s.p.a., Italy.
    - Sara Vinco, *"Reuse and integration of heterogeneous components for efficient embedded software generation"*, Graduation date: May 2013. Current position: Assistant professor at Politecnico di Torino, Italy.

  - Luigi Di Guglielmo, *"Realizability of embedded controllers: from hybrid models to concrete implementations"*, Graduation date: May 2012. Current position: R&D Engineer at ALES s.r.l., Italy.
  - Giuseppe Di Guglielmo, *"On the validation of embedded systems through functional ATPG"*, Graduation date: April 2009. Current position: Associate research scientist, Columbia University of NY, USA.
  - Nicola Bombieri, *"A TLM design for verification methodology"*, Graduation date: March 2008. Current position: Associate professor at Università degli Studi di Verona, Italy.
  - Cristina Marconcini, *"A Functional ATPG as a bridge between validation and testing"*. Graduation date: March 2008. Current position: Product manager at STMProducts s.r.l., Italy.
- Advising of 15 research fellows at University of Verona, Italy.
- Advising of more than 100 between undergraduate and graduate student thesis in the field of embedded systems and operating systems at Università degli Studi di Verona, Italy. In this context, Graziano Pravadelli participated in more than 20 graduation commissions.

12. Institutional activity

Graziano Pravadelli has served at University of Verona in the following roles:

- President of the Quality Assurance Board (Presidio della Qualità) since July 2017.
- Member of the Quality Assurance Board (Presidio della Qualità), February 2016 - June 2017.
- President of the self-evaluation commission and responsible for AVA (Autovalutazione, Valutazione periodica, Accreditamento) of the master course on Computer Science and Engineering (from 2014 to February 2016), in charge of managing the quality assurance procedures in accordance with the AVA system introduced with the Italian Law 20/12/10 n. 240.
- President of the self-evaluation commission and AVA responsible of the bachelor course on Computer Science (from 2011 to 2014), in charge of managing the quality assurance procedures in accordance with the AVA system introduced with the Italian Law 20/12/10 n. 240.
- President of the self-evaluation commission of the bachelor course on Computer Science (from 2009 to 2010), in charge of managing the quality assurance procedures and the redaction of the *Rapporto di Autovalutazione* (RAV).
- President of the Comitato Area CIVR 09 (from 2008 to 2010).
- Delegate of the Teaching Staff Council for the PhD degree in Computer Science at the Graduate School of Science Engineering and Medicine (from 2007 to 2009).

Since July 2015, Graziano Pravadelli is part of the Albo "Esperti della Valutazione – Profilo Esperti Disciplinari" of the Italian National Agency for the Evaluation of Universities and Research Institute (ANVUR) for the 09 Area. In this role he served as:

- Coordinator of the commission of experts for the initial accreditation of 6 bachelors and 4 masters in 2017;
- Member of the commission of experts for the initial accreditation of 1 bachelor in 2017;
- Member of the commission of experts for the initial accreditation of 4 masters in 2018;
- Member of the commission of experts for the periodic accreditation of the Università degli Studi di Ferrara in 2016;
- Member of the commission of experts for the periodic accreditation of the Università degli Studi di Cassino e del Lazio Meridionale in 2017;
- Member of the commission of experts for the periodic accreditation of the Università degli Studi di Genova in 2018.

13. Transfer of technology

Graziano Pravadelli is co-founder and co-owner of EDALab s.r.l. (http://www.edalab.it), an Italian SME whose mission consists of giving support for innovation and technology transfer in embedded system modeling and verification. EDALab was founded on July 16, 2007 and it currently employs 13 persons in the development of embedded SW, and the design of CAD tools for modelling and verification of networked embedded systems. EDALab has been involved in several industrial and scientific projects (including the EU projects CONTREX, COMPLEX, SMAC and COCONUT) in cooperation with international companies (e.g., STMicroelectronics, Philips, Keysight - Agilent, Exor International, On semiconductor), universities (e.g., University of Paderborn, Polytechnic of Turin, Polytechnic of Milan, University of Cantabria), and research centres (e.g., FBK, OFFIS).

Among EDALab's main products, HIFSuite and radCHECK found their scientific basis on the research activity of Graziano Pravadelli.

In July 2017 Graziano Pravadelli has started the launch of IF's - ICT for families, a startup, currently in its incubation phase within the University of Verona, for the development of ICT-based virtual coaching systems where embedded systems are used to support persons with physical and cognitive impairments. IF's -ICT for families won the Special mention "Best National Social Innovation Project" at "Premio Nazionale per l'Innovazione 2017 (National Prize for Innovation)" on December 01, 2017.

14. Publications

14.1 International journals

1. L. Piccolboni, A. Menon, G. Pravadelli, Efficient Control-Flow Subgraph Matching for Detecting Hardware Trojans in RTL Models, «ACM Transactions on Embedded Computing Systems», vol 16, n.5, 2017, pp. 137:1-137:19.
2. D. Ferraretto, G. Pravadelli, Simulation-based fault injection with QEMU for speeding-up dependability analysis of embedded software, «Journal of Electronic Testing: Theory and Applications», vol 32, n.1, 2016, pp. 43-57.
3. N. Bombieri, F. Fummi V. Guarnieri, G. Pravadelli F. Stefanni; T. Ghasempouri, M Lora, G. Auditore, M. Negro Marcigaglia, Reusing RTL assertion checkers for verification of SystemC TLM models, «Journal of Electronic Testing: Theory and Applications» , Vol. 31, n.2, 2015 , pp. 167-180.
4. N. Bombieri, F. Fummi, V. Guarnieri. G. Pravadelli, Testbench qualification of SystemC TLM protocols through Mutation Analysis. «IEEE Transactions on Computers». Vol. 63, n.5, 2014, pp. 1248-1261.
5. G. Di Guglielmo, L. Di Guglielmo, A. Foltinek, M. Fujita, F. Fummi, C. Marconcini, G. Pravadelli. On the integration of model-driven design and dynamic assertion-based verification for embedded software. «The Journal of Systems and Software» , vol. 86 , 2013 , pp. 2013-2033.
6. L. Di Guglielmo, F. Fummi, G. Pravadelli, F. Stefanni, S. Vinco. UNIVERCM: The UNIversal VERsatile Computational Model for Heterogeneous System Integration. «IEEE Transactions on Computers» , vol. 62 , 2013 , pp. 225-241.
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9. N. Bombieri, F. Fummi, G. Pravadelli. Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions. «IEEE Transactions on Computers», vol. 60 , n. 12 , 2011 , pp. 1730-1743.
10. G. Di Guglielmo, L. Di Guglielmo, F. Fummi Franco, G. Pravadelli. Efficient Generation of Stimuli for Functional Verification by Backjumping Across Extended FSMs. «Journal of Electronic Testing: Theory and Applications», vol. 27 , n. 2 , 2011 , pp. 137-162.
11. N. Bombieri, M. Ferrari, F. Fummi, G. Di Guglielmo, G. Pravadelli, F. Stefanni, A. Venturelli. HIFSuite: Tools for HDL Code Conversion and Manipulation. «Eurasip Journal On Embedded Systems», vol. 2010, n. 10.1155/2010/436328, 2010, pp. 1-20.

12. F. Fummi, M. Loghi, M. Poncino, G. Pravadelli. A Co-Simulation Methodology for HW/SW Validation and Performance Estimation. «ACM Transactions on Design Automation of Electronic Systems», vol. 14, n. 2, 2009, pp. 23:1-23:32.
13. N. Bombieri, F. Fummi, G. Pravadelli. Reuse and Optimization of Testbenches and Properties in a TLM-to-RTL Design Flow. «ACM Transactions on Design Automation of Electronic Systems», vol. 13, n. 3, 2008, pp. 47:1-47:22.
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18. M. Loghi, T. Margaria, G. Pravadelli, B. Steffen. Dynamic and Formal Verification of Embedded Systems: A Comparative Survey. «International Journal of Parallel Programming», vol. 33, n. 6, 2005, pp. 585-611.
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20. F. Ferrandi, F. Fummi, G. Pravadelli, D. Sciuto. Identification of Design Errors through Functional Testing. «IEEE Transactions on Reliability», vol. 52, n. 4, 2003, pp. 400-412.

14.2 International conferences

1. F. Demrozi, K. Costa, F. Tramarin, G. Pravadelli. A graph-based approach for mobile localization exploiting real and virtual landmarks. In “IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)”, Verona, Italy, 8-10 October, 2018.
2. A. Danese, V. Bertacco, G. Pravadelli. Symbolic assertion mining for security validation. In “ACM/IEEE Design automation and Test in Europe (DATE)”, Dresden, Germany, 19-23 March 2018.
3. A. Danese, G. Pravadelli, V. Bertacco. DOVE: pinpointing firmware security vulnerabilities via symbolic control flow assertion mining (work-in-progress). In “ACM/IEEE International Conference Hardware/Software Codesign and System Synthesis (CODES+ISSS)”, Seoul, Korea, 10-15 October 2017.
4. A. Danese, N. Dalla Riva, G. Pravadelli. A-TEAM: Automatic Template-based Assertion Miner. In “ACM/IEEE Design Automation Conference (DAC)”, Austin, TX, USA, 18-22 June 2017.

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8. D. Yunge, S. Park, P. Kindt; G. Pravadelli, S. Chakraborty. Dynamic Service Synthesis and Switching for Medical IoT and Ambient Assisted Living. In "IEEE International High Level Design Validation and Test Workshop (HLDVT)", Santa Cruz, USA, 7-8 October 2016.
9. L. Piccolboni, G. Pravadelli. Stimuli Generation through Invariant Mining for Black-Box verification. In "IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC)", Tallinn, Estonia, 26-28 September, 2016.
10. A. Danese, G. Pravadelli, I. Zandonà. Automatic generation of power state machines through dynamic mining of temporal assertions. In ACM/IEEE Design automation and Test in Europe (DATE), Dresden, Germany, 14-18 March 2016.
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15. A. Danese, T. Ghasempouri, G. Pravadelli, Automatic extraction of assertions from execution traces of behavioural models. In ACM/IEEE Design automation and Test in Europe (DATE), Grenoble, France, 9-13 March 2015.
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17. D. Ferraretto, G. Pravadelli, Efficient fault injection in QEMU. In IEEE Latin American Test Symposium (LATS), 25-27 March 2015.

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26. L. Di Guglielmo, F. Fummi, G. Pravadelli, F Stefanni, S. Vinco. A Formal Support for Homogeneous Simulation of Heterogeneous Embedded Systems. In "IEEE International Symposium on Industrial Embedded Systems", Karlsruhe, Germany, 20-22 June 2012.
27. G. Di Guglielmo, G. Pravadelli. A testbench specification language for SystemC Verification. In "IEEE International Conference on Hardware/Software Codesign and System Synthesis" , Tampere, Finland, 7-12 October 2012 , pp. 333-342.
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Graziano Pravadelli is co-author of the book chapter (in Italian):

- D. Botturi, F. Fontana, G. Pravadelli, ”Appendice A: Laboratorio di Linux”, in V. Manca *“Metodi Informazionali”*, Bollati Boringhieri 2003, pp. 129-206.

Graziano Pravadelli translated from English to Italian with Prof. Alfredo Petrosino the book:

- D.M. Dhamdhere, “*Operating systems. A concept based approach*”, McGraw-Hill, 2008.

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Graziano Pravadelli translated from English to Italian the following book chapters:

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Graziano Pravadelli revised the following books:

- D.M. Dhamdhere, "*Operating systems. A concept based approach*", McGraw-Hill International Edition 2003.
- A. Bellini, A. Guidi, "*Linguaggio C - Guida alla programmazione*", McGraw-Hill 2006.

Verona, October 1, 2018

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In compliance with the GDPR and the Italian Legislative Decree no. 196 dated 30/06/2003, I hereby authorize you to use and process my personal details contained in this document.

Graziano Pravadelli

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