Forum on specification & Design Languages

- **Location**
  - The symposium will take place at the "Accademia di Agricoltura Scienze e Lettere" (Agriculture, Science and Literature Academy) in the city center of Verona. Further information: http://www.aaslvr.it
- **Welcome Reception**
  - We kindly invite all participants to a Welcome Reception on Monday, September 18th at 6:30 p.m.. The reception will take place at the Osteria Canton, piazza delle Erbe 36.
- **Social Event**
  - On Tuesday, September 19th at 8:30 p.m., all participants are invited to Re Teodorico restaurant: http://reteodorico.com. While having a beautiful view of Verona by night, we will serve a dinner and we invite everyone to have a nice summer evening with us. During this, contacts to other participants can be strengthened and the day is concluded in a relaxed atmosphere.
    The social event will start at 6:30 p.m. (Piazza Brà). We collect all attendees at the "Accademia" for the visit of the best historical sites of Verona. We will then arrive to the funicular of Castel San Pietro, that we will use for reaching the restaurant.
- **Most up-to-date information**
  - http://fdl17.di.univr.it

IEEE CEDA® IEEE Council on Electronic Design Automation

IFIP WORKING GROUP 10.5 Design and Engineering of Electronic Systems

UNIVERSITÀ di VERONA Dipartimento di INFORMATICA

ecsi electronic chips & systems design initiative

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- **Keynote 1**
  - *IoT trends and innovative applications* - Roberto Zafalon, STMicroelectronics
    The keynote will tackle with the three major IoT challenges today: interoperability, security, and business model (monetization). The strong enabling technologies roots (i.e. semiconductor and IP Design) will set the stage for a comprehensive view of the key IoT end-markets and of the most innovative applications expected to boost the massive deployment of IoT by the next 4 years.
- **Keynote 2**
  - *Programming in a Heterogeneous World* - Jan Kuper, QBayLogic
    This talk will argue that translation mechanisms from well known and well developed programming methodologies into low-level platform specific programming is doomed to fail because the way each type of computing platform deals with its internal space and time in a different way. Instead, we will argue that we should start from a really platform independent level, for which mathematics is a good candidate.
- **Keynote 3**
  - *Cyber Security of cyber physical critical infrastructure* - Sandeep Shukla, IIT Kanpur
    In this talk we will explore this question, and we will show that there is indeed benefit in taking approaches based on formalized languages for system specification, or system design, not only for analyzability at various abstraction levels of risk, and visibility of attack vectors but also for better comprehension of systemic risks, guiding resilient design of system architecture, and budgeting resources in optimal manner.

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September 18-20 | Verona, Italy

Final PROGRAM

FDL Forum on specification & Design Languages

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Monday 18

- 08:30 AM-09:00 AM Registration
- 09:00 AM-10:30 AM **Hands-on Tutorial 1**
  - *HIFSuite for Cyber-physical VPs generation*
    - Michele Lora, Univ. of Verona / EDALab
- 10:30 AM-11:00 AM Coffee break
- 11:00 AM-12:30 PM **Hands-on Tutorial 2**
  - *The SPARK 2014 programming language*
    - Martin Becker, Technical Univ. of Munich
- 12:30 PM-01:30 PM Lunch
- 01:30 PM-02:00 PM **Opening remarks**
  - Franco Fummi, Univ. of Verona
  - Hiren Patel, Univ. of Waterloo
  - Graziano Pravadelli, Univ. of Verona
- 02:00 PM-03:00 PM **Keynote 1**
  - *IoT trends and innovative applications*
  - Roberto Zafalon, STMicroelectronics
- 03:00 PM-03:30 PM Coffee break
- 03:30 PM-05:00 PM **Session 1**
  - *Modeling and Simulation*
    - Chair: Julio Medina, Univ. of Cantabria
    - 1.1 Fault Analysis in Linear Analog Circuits through Language Manipulation and Abstraction
      - Enrico Fraccaroli, Univ. of Verona - Francesco Stefanni, EDALab - Franco Fummi, Univ. of Verona - Mark Zwolinski, Univ. of Southampton
    - 1.2 Actor Fission Transformations for Executing Dataflow Programs on Manycores
      - Essayas Gebrewahid, Halmstad Univ. - Zain Ul-Abdin, Halmstad Univ.
    - 1.3 Rethinking of I/O-Automata Composition
      - Sarah Chabane, Univ. M'hamed Bougara - Rabea Ameur-Boulifa, Université Paris-Saclay - Mohamed Mezghiche, Univ. M'Hamed Bougara
- 05:00 PM-06:00 PM **Panel 1**
  - *The WHAT? and WHY? of high-level languages in designing and verifying complex integrated systems*
    - Moderator: Sara Bocchio, STMicroelectronics
    - Nigel Woolaway, Leading Edge
    - Daniel Große, Univ. of Bremen
    - Massimo Roselli, Cadence Design Systems
- 06:00 PM-07:00 PM Welcome reception

Tuesday 19

- 08:30 AM-09:30 AM **Keynote 2**
  - *Programming in a Heterogeneous World*
  - Jan Kuper, QBayLogic
- 09:30 AM-11:00 AM **Session 2**
  - *Languages and Design Methods for Time-critical Systems*
    - Chair: Daniel Große, Univ. of Bremen
    - 2.1 Real-Time Ticks for Synchronous Programming
      - Reinhard von Hanxleden, Kiel Univ. - Timothy Bourke, INRIA, PARKAS Team - Alain Girault, INRIA, SPADES Team
    - * 2.2 Symbolic Simulation of Dataflow Synchronous Programs with Timers
      - Guillaume Baudart, IBM Research - Timothy Bourke, Inria/ENS - Marc Pouzet, LIENS
    - 2.3 Compositional Timing-Aware Semantics for Synchronous Programming
      - Joaquin Aguado, Univ. of Bamberg - Michael Mendler, Univ. of Bamberg - Jia Jie Wang, Univ. of Auckland - Bruno Bodin, Univ. of Edinburgh - Partha Roop, Univ. of Auckland
- 11:00 AM-11:30 AM Coffee break
- 11:30 AM-01:00 PM **Session 3**
  - *Programming Languages for Quantum Computing*
    - Chair: Mathias Soeken, EPFL
    - 3.1 Benoit Valiron, CentraleSupelec, Univ. Paris-Saclay
    - 3.2 Nader Khammassi, TU Delft
    - 3.3 Michael Kirkedal Thomsen, Univ. of Copenhagen
- 01:00 PM-02:00 PM Lunch
- 02:00 PM-03:00 PM **Panel 2**
  - *Languages for CPS: Are they needed?*
    - Moderator: Nicola Bombieri, Univ. of verona
    - Julio Medina, Univ. de Cantabria
    - Sandeep Shukla, IIT Kanpur
    - Reinhard von Hanxleden, Kiel Univ.
- 03:00 PM-04:00 PM **WiP Session + Posters**
  - Chair: Graziano Pravadelli, Univ. of Verona
  - WiP1 Error Propagation for Cascading Metamodels Applied on an Electric Drive Application
    - Christine Forster, Infineon - Manuel Harrant, Infineon - Jerome Kirscher, Infineon - Linus Maurer, Univ. der Bundeswehr München - Georg Pelz, Infineon
  - WiP2 From SQL to Database Processors: A Retargetable Query Planner
    - Arda Yurdakul, Bogazici Univ.
  - WiP3 Towards MARTE++: An Enhanced UML-based Language to Model and Analyse Real-Time and Embedded Systems for the IoT Age
    - Julio L. Medina, Univ. de Cantabria - Eugenio Villar, Univ. de Cantabria
  - WiP4 Scalar Replacement with Array Dataflow Analysis for Hardware Synthesis
    - Kenshu Seto, Tokyo City Univ.
- 04:00 PM-04:30 PM Coffee break
- 04:30 PM-06:00 PM **Session 4**
  - *Design and Validation Methodologies*
    - Chair: Tom Kazmierski, Univ. of Southampton
    - * 4.1 Automatic Generation of Cycle-Accurate Simulink Blocks from HDL IPs
      - Stefano Centomo, Univ. of Verona - Michele Lora, Univ. of Verona - Antonio Portaluri, EDALab - Francesco Stefanni, EDALab - Franco Fummi, Univ. of Verona
    - 4.2 Towards Consistency Checking Between HDL and UPF Descriptions
      - Arthur Kalsing, TIMA Laboratory - Laurent Fesquet, TIMA Laboratory - Chouki Aktouf, Defacto Technologies
    - * 4.3 Towards Early Validation of Firmware-Based Power Management Using Virtual Prototypes: A Constrained Random Approach
      - Vladimir Herdt, Univ. of Bremen - Hoang M. Le, Univ. of Bremen - Daniel Große, Univ. of Bremen & DFKI - Rolf Drechsler, Univ. of Bremen & DFKI
- 06:00 PM-10:00 PM Social Event

Wednesday 20

- 08:30 AM-09:30 AM **Keynote 3**
  - *Cyber Security of cyber physical critical infrastructure*
  - Sandeep Shukla, IIT Kanpur
- 09:30 AM-11:00 AM **Session 5**
  - *Next generation many-cores*
    - Chair: Nicola Bombieri, Univ. of Verona
    - 5.1 Language and Hardware Acceleration Backend for Graph Processing
      - Andrey Mokhov, Newcastle Univ.- Alessandro de Gennaro, Newcastle Univ. - Ghaith Tarawneh, Newcastle Univ. - Jonny Wray, e-Therapeutics - Georgy Lukyanov, Newcastle Univ. - Sergey Mileiko, Newcastle Univ. - Joe Scott, Newcastle Univ. - Alex Yakovlev, Univ. of Newcastle - Andrew Brown, Univ. of Southampton
    - 5.2 Runtime Task Mapping for Lifetime Budgeting in Many-Core Systems
      - Liang Wang, The Chinese Univ. of Hong Kong - Xiaohang Wang, South China Univ. of Technology - Ho-fung Leung, The Chinese Univ. of Hong Kong - Terrence Mak, Univ. of Southampton
    - 5.3 A Reconfigurable Bit-serial FFT/FIR Processor for Ultra-low-power Applications
      - Yue Lu, Univ. of Southampton - Tom Kazmierski, Univ. of Southampton
- 11:00 AM-11:30 AM Coffee break
- 11:30 AM-01:00 PM **Session 6**
  - *Design, Optimization, and Verification of Modern Industry Applications*
    - Chair: Ashraf Salem, Mentor Graphics
    - 6.1 Identifying Bottlenecks in Manufacturing Systems Using Stochastic Criticality Analysis
      - João Bastos, Eindhoven Univ. of Technology - Bram van der Sanden, Eindhoven Univ. of Technology - Olaf Donk, ICT Group - Jeroen Voeten, Eindhoven Univ. of Technology - Sander Stuijk, Eindhoven Univ. of Technology - Ramon Schiffelers, Eindhoven Univ. of Technology - Henk Corporaal, Eindhoven Univ. of Technology
    - 6.2 ASIL Decomposition Using SMT
      - Mona Safar, Ain Shams Univ.
    - 6.3 Multi-Objective Optimization-based Development of Power Electronics for Automotive Applications
      - Jonas Stricker, Universität der Bundeswehr München - Benno Köppl, Infineon Technologies - Jérôme Kirscher, Infineon Technologies - Thomas Nirmaier, Infineon Technologies - Linus Maurer, Universität der Bundeswehr München - Georg Pelz, Infineon Technologies
    - 6.4 An Emulation Framework for Closed Source Components in Multi-core Automotive Platforms
      - Ignacio Sañudo, Univ. of Modena and Reggio Emilia - Paolo Burgio, Univ. of Modena and Reggio Emilia - Marko Bertogna, Univerity of Modena
- 01:30 PM-3:00 PM Lunch and closing

** Best paper award nomination*