Low Power and Reliable Design for Emerging Tecnologies

Abstract: As the technology node continuously scales down, Moore's law may not be sustainable as before for conventional CMOS technology. To deal with this challenge, several emerging memory technologies have been proposed as promising cadidates of SRAM. Among them, spintronic and carbon nanotube devices have unique desirable merits, such as non-volatitliy, fast access speed, high endurance, ultra low leakage power and compatiblity with CMOS process. Therefore, they are promising cadidates for next generation of logic and memory design. On the other hand, since the fabrication processes of STT-MRAM and carbon nanotube devices are not mature yet, it is imperative to enhance the reliability and the energy efficiency from both circuit level and architecture level perspectives to guarantee the commercial success of these emerging technologies.

In this talk, I will introduce my group's several relevant work on low power and reliability design of STT-MRAM and carbon nanotube based memory. During this talk, I will also briefly introduce Beihang University and expect to establish the

collaborations with University of Verona.

Bio: Dr. Cheng got his Ph.D. degree from Institute of Comupting Technology, Chinese Academy of Sciences in 2012. Then, he spent one year at CNRS/LIRMM laboratory, Montpellier, France. At the end of 2013, he joined EE department of Beihang University as an assistant professor. During 2015 – 2016, he went to University of California, Santa Barbara, U.S. as a visiting scholar. His research topic includes low power and reliability design for 3D integerated circuits, low power and reliability design for emerging memory technologies, especially STT-MRAM and carbon nanotube devices. He has co-authored more than 30 peer-reivewed papers. He is a member of IEEE/ACM, a senior member of CCF (China Computing Federation), and is the TPC member of 2018 IEEE/ACM DATE conference, 2018 IEEE PATMOS conference and 2018 IEEE ISVLSI conference. He is also the technical reviewer of IEEE Trans. on VLSI, IEEE Trans. on CAD and IEEE Trans. on Reliability.