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Short introduction

Nicola Bombieri received the PhD in Computer Science from the University of Verona in 2008. Since then, he is Assistant Professor at the Department of Computer Science, University of Verona.

Research

His main research activity focuses on parallel and heterogeneous architectures, parallel computing, and parallel programming languages. He develops strategies to parallelize software applications for multi-core and many-core architectures targeting performance, power, and energy consumption design constraints. His research field also includes electronic design automation (EDA) applied to Smart Systems modeling and verification, automatic generation of embedded parallel software, hardware description languages (HDLs), EDA applied to Systems Biology for network modeling and simulation.

He serves as Technical Program Committee member, General Chair for Workshops/Special sessions, Session Chair, Keynote Chair at ACM/IEEE conferences like MCSoC, SIES, ECSI FDL, CODES/ISSS, MEMOCODE, DSD, VLSI-SoC, ETS.

He has been involved in 6 FP6/FP7 European Projects and several national FSE/Joint Projects as Project and Technical Manager.

In the last 5 years, he has been author of 27 conference papers and 16 Journal articles.

He founded and is head of the *PARCO Lab* at the Department of Computer Science, University of Verona. The *PARCO Lab*, which goal is the research and development of advanced parallel programming techniques for CPU/GPU architectures has been awarded by NVIDIA Corporation and, currently, it hosts 5 PhD students, 1 PostDoc, 3 Master students, and 8 intern students (for bachelor and master degree stage). The *PARCO Lab* serves as multidisciplinary research laboratory for applying advanced and parallel architectures to Bioinformatics, Systems Biology, Molecular Biology, Robotics, Artificial Intelligence, and Embedded Systems design and verification in collaboration with national and international research groups.

Employment

Since 2008: Assistant Professor at the Department of Computer Science, University of Verona, Italy.
Since 2008: R&D consultant at EDALAB s.r.l., Verona, Italy

Research activity

Nicola Bombieri began his research activity in 2005, by studying transaction level modeling (TLM) in the field of modeling and simulation of embedded systems under the supervision of Prof. Fummi at the Department of Computer Science, University of Verona and in collaboration with STMicroelectronics s.r.l., Milan, Italy. In 2006, he introduced the concept of *automatic abstraction*

from register-transfer level (RTL) to TLM to accelerate system model simulation. The proposed automatic abstraction methodology has been implemented in a commercial tool and is currently one of the most referenced solutions for reusing existing RTL IPs into TLM systems via abstraction.

He introduced the theory of event-based equivalence checking between RTL-TLM models at the University of Southampton (UK) in collaboration with Prof. Joao P. Marques-Silva in 2007. He proposed a methodology for RTL-TLM automatic transactor generation (which has been best paper candidate at ACM/IEEE DATE) in 2008, the concept of mutation analysis applied to TLM verification (which has been best paper candidate at ACM/IEEE DATE) in 2009, and the abstraction of SystemC data types for accelerating system simulation (which received the best paper award at ECSI/IEEE FDL) in 2011. He worked on the reuse of RTL IPs at the Columbia University (NY) in collaboration with Prof. L. Carloni in 2011 and 2012.

In 2011, he funded and since then he is principal investigator of the parallel architecture research group at the Department of Computer Science, University of Verona. His research focuses on parallel and heterogeneous architectures, parallel computing, and parallel programming languages. He has been developing strategies to parallelize software applications for multi-core and many-core architectures targeting performance, power, and energy consumption design constraints.

With his former PhD student, since 2013, he developed parallel techniques for graph traversal and analysis (breadth-first search and single source shortest path) through GPU computing. He also gave an important contribution to the state of the art of the load balancing techniques for GPU applications. The three contributions and the corresponding open-source implementations are currently and increasingly adopted as building blocks for many GPU applications in different research fields worldwide. They are the most efficient in terms of performance and work complexity at the state of the art.

He worked on the parallel implementation of graph decomposition into strongly connected components (SCC problem) for GPUs in collaboration with M. Ceska (Oxford University, UK) and J. Barnat (Masaryk University, CZ). He worked on the parallelization of the sub-graph isomorphism algorithm and its implementation for multi-core architectures in collaboration with D. Sasha (New York University, NY) and A. Ferro (University of Catania). He worked on the parallelization of the approximate graph querying and bucket elimination problems, in collaboration with A. Pulvirenti (University of Catania) and A. Farinelli (University of Verona), respectively. He developed a performance model based on microbenchmarking for GPU applications in collaboration with F. Fummi (University of Verona). He applied GPU parallel computing in the filed of embedded system design and verification, in collaboration with F. Fummi and G. Pravadelli (University of Verona).

Since 2014, he is working on modeling and simulation of biological systems through EDA methodologies and tools. In particular, he studies emerging properties through qualitative modeling of the intracellular signalling network controlling integrin activation mediating leukocyte recruitment from the blood into the tissues, in collaboration with C. Laudanna (Department of Medicine, University of Verona). He has applied his modeling and simulation framework for the robustness and sensitivity analysis of the Colitis-associated Colon Cancer (CAC) network and, more recently, for the analysis of the drug combinations that target the mitochondria in leukemia, in collaboration with G. Bader (Toronto University, CA).

Research services

He serves as referee to several journals such as IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Embedded Computing Systems, ACM Transactions on Design Automation of Electronic Systems, IEEE Transactions on VLSI, IEEE Transactions on Computer-aided design of ICS, IEEE Design and Test of Computer, Elsevier Parallel Computing, IEEE Transactions on Computers and conferences such as ACM/IEEE DAC, ACM/IEEE DATE, ACM/IEEE CODES, IEEE ICCAD, IEEE ETS, IEEE FDL, IEEE HLDVT, ACM/IEEE MEMOCODE, IEEE VLSI-SOC.

Organization of scientific meetings and conference committee participation

He served as:

- Keynote Chair, Special Session organizer, Special Session Chair at IEEE/ECSI Forum on specification and Design Languages (FDL) 2016, Bremen (Germany), 14-16 September 2016.
- Session Chair at IEEE International Symposium on Industrial Embedded Systems (SIES). Krakow (Poland), 23-25 May 2016.
- Technical Program Committee member of IEEE/ECSI Forum on Specification and Design Languages (FDL) 2016. Bremen (Germany), 14-16 September 2016
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES) 2016. Krakow (Poland), 23-25 May 2016.
- General Chair for the Workshops/Special Sessions at IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC) 2015, Turin, Italy, 23-25 Sept. 2015.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES). Siegen (Germany), 8-10 June 2015.
- Hands-on tutorial co-organizer and speaker at ACM/IEEE Embedded Systems Week (CODES/ISSS) 2014. Title: Methods and tools for smart device integration and simulation. New Delhi – India. 12-17 Oct. 2014.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems – Work in Progress (SIES-WiP). Pisa (Italy), 18-20 June 2014.
- Technical Program Committee member of IEEE International Symposium on Industrial Embedded Systems (SIES). Pisa (Italy), 18-20 June 2014.
- Technical Program Committee member of IEEE Euromicro Conference on Digital System Design (DSD) Cesme, Izmir- Turkey, 5-8 September 2012.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2011. Hong-Kong (China), 3-5 October, 2011.
- Technical Program Committee member of IEEE International Conference on Very Large Scale Integration (VLSI-SOC), 2010. Madrid (Spain), 27-29 September 2010.
- Session Chair at ACM/IEEE International Conference on Formal Methods and Models for System Design (MEMOCODE) 2010. Grenoble (France), 26-28 June, 2010.
- Session Chair at IEEE European Test Symposium (ETS) 2009. Sevilla (Spain), 25-29 May, 2009.

European Project participations

He had technical and scientific participation in the following FP7 European Projects:

- TOUCHMORE: Automatic Customizable Tool-chain for heterogeneous Multicore Platform Software Development (FP7-ICT-2011-7-288166). Starting date: 01/09/2011. Duration: 30 months. Role: Project Manager.
- SMAC: Smart Systems Co-design (FP7-ICT-2011-7-288827). Starting date: 01/10/2011. Duration: 36 months. Role: Project Manager.
- COMPLEX: Codesign and Power Management in Platform-based Design-space Exploration (FP7-ICT-2009-4-247999). Duration 36 months. Role: Project Manager.
- COCONUT: A Correct-by-Construction Workbench for Design and Verification of Embedded Systems (FP7-2007-IST-1-217069). Starting date: 01/11/2008, Duration: 30 months. Role: Technical Manager.
- VERTIGO: Verification and Validation of Embedded System Design workbench (FP6-2005-IST-5-033709). Starting date: 01/01/2006. Duration: 30 months. Role: Technical Manager.
- CREDES: Centre of Reserach Excellence in Dependable Embedded Systems (FP7-REGPOT-2008-1). Starting date: 01/10/2009. Duration: 36 months. Role: Technical Manager.

National project participations

- H2S: Framework per la generazione automatica di SW embedded tramite riuso di modelli RTL esistenti. (FSE Project, 2011). Duration 12 months. Role: Principal Investigator.

- OPTIMUM: OPTImizing dependability via MUtation analysis for Microelectronics (Joint Project di Ateneo, 2007). Starting date: 01/01/2011. Duration: 12 months. Role Technical Manager.
- EFFORT: Ambiente basato su EFSM per la progettazione e la verifica di software embedded (Joint Project di Ateneo, 2007). Starting date: 01/01/2008. Duration: 30 months. Role: Technical Manager.

Other research activities

He founded and is head of the *PARCO Lab* at the Department of Computer Science, University of Verona. The *PARCO Lab*, which goal is the research and development of advanced parallel programming techniques for CPU/GPU architectures:

- Has been awarded as *GPU Research Center* from NVIDIA Corporation and funded with Tesla K40 devices;
- Currently hosts 5 PhD students, 1 PostDoc, 3 Master students, and 14 intern students (for bachelor and master degree stage);
- Serves as multidisciplinary research laboratory for applying parallel architectures to:
  - Bioinformatics (with Prof. D. Shasha, Department of Computer Science - New York University-NY, Prof. A. Ferro, Department of Clinical and Experimental Medicine – University of Catania).
  - Systems Biology (with Prof. G. Bader, Department of Molecular Genetics – University of Toronto-CA, Prof. C. Laudanna, Department of Medicine – University of Verona).
  - Molecular Biology (with Dr. A. Giorgetti, Department of Biotecnology – University of Verona).
  - Robotics and Artificial Intelligence (with Prof. A. Farinelli, Dr. R. Muradore, Department of Computer Science – University of Verona)
  - Embedded Systems Design and Verification (with Prof. G. Pravadelli, Prof. F. Fummi, Department of Computer Science – University of Verona).

Academic and research experience at foreign institutions

He has been visiting researcher at

- Columbia University in the city of New York (NY), USA (Computer Science Department) from 01/August/2011 to 31/October/2011.
- Columbia University in the city of New York (NY), USA (Computer Science Department) from and from 15/May/2012 to 30/June/2012.
- University of Southampton - Electronics and Computer Science, UK from Sept/2006 to Feb/2007.

Supervision of Graduate Students, Postdoctoral fellows, PhD students

He is/has been Tutor of 2 PhD Students, Committee Member of 8 PhD Students, Tutor of 13 Master students, Co-tutor of 18 Master students, Tutor of 15 Bachelor students, Supervisor of 2 PosDocs,

Grants, Awards, and selected invited talk

Sept 2016: Talk at Italian Workshop on Embedded Systems (IWES) – Pisa. “An EDA Platform for Modeling and Simulation in Systems Biology”.

July 2016: Advanced course at GEVIS Visual Inspection Systems s.r.l. “Parallel programming for GPU architectures with OpenCL and OpenACC” (18 hours), Fidenza (PR), Italy.

June 2016: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) for the project “Integrating national and international spontaneous adverse drug reaction knowledge bases for pattern discovery in pharmacovigilance”.

June 2015: Grant from GNCS (Gruppo Nazionale per il Calcolo Scientico) to participate to the ISMB/ECCB conference, 2015.

June 2014: Grant from Microsoft Corporation for the project “Italian MSDN Library content for Visual Studio 2013”.

May 2014: Advanced course at QR/Newtom s.r.l. “OpenCL and parallel programming for GPU architectures” (14 hours). Verona, Italy.

June 2013: Invited talk at Intel Corporation® - Hillsboro, Oregon – USA. “On the automatic abstraction of RTL IPs into SystemC TLM models.

February 2013: Invited talk at Embedded World Conference 2013. “Automatic HDL conversion and abstraction methodologies”. Nuremberg – Germany.

October 2012: Invited talk at STMicroelectronics s.r.l. – Catania- Italy. “A2T: Automatic abstraction of RTL IPs into TLM models”.

Sept. 2012: Grant from Microsoft Corporation for the project “Italian MSDN Translation Wiki 2012”.

February 2012: Cooperint Grant from the University of Verona for joining the Department of Computer Science - Columbia University in the City of New York as visiting scholar. Project title: "Advancements on improving design space of RTL IP logic synthesis through abstraction and high-level synthesis".

November 2011: Invited talk at ESA-European Space Agency-Italy (web seminar) “Accelerating RTL simulation through RTL-TLM abstraction”

September 2011: Best paper Award at IEEE/ECSI Forum for Design Languages (FDL)", Oldenburg, Germany,13-15 September, 2011, with the paper: N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco,"Efficient Implementation and Abstraction of SystemC Data Types for Fast Simulation".

August 2011: Cooperint Grant from the University of Verona for joining the Department of Computer Science - Columbia University in the City of New York as visiting scholar. Project title: "Improving design space of RTL IP logic synthesis through abstraction and high-level synthesis".

April 2011: Invited talk at Synopsys Inc. (web seminar) “Accelerating RTL simulation through RTL-TLM abstraction”

April 2009: Invited paper N. Bombieri, F. Fummi, G. Pravadelli, M. Hampton, F. Letombe, "Functional qualification of TLM verification" at ACM/IEEE Design, Automation and Test in Europe (DATE) , Nice, France , 20-24 April, 2009.

March 2008: Best paper candidate in the track “Verification & Low Power Design at ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, with the paper: N. Bombieri, F. Fummi, G. Pravadelli, "A Mutation Model for the SystemC TLM 2.0 Communication Interfaces".

March 2008: Best paper candidate in the track “Verification & Low Power Design at ACM/IEEE Design, Automation and Test in Europe (DATE)", Munich, Germany, 10-14 March, 2008, with the paper: N. Bombieri, N. Deganello, F. Fummi, "Integrating RTL IPs into TLM Designs Through Automatic Transactor Generation".

June 2007: SIGDA grant for attending the PhD Forum at the ACM/IEEE Design Automation Conference (DAC’07) conference, San Diego, CA – USA.

June 2007: Invited talk at the “Third national conference of Logic Synthesis”, University of Verona, Italy.

June 2007: Invited talk at the Department of Electronic Engineering, University of Udine (Italy). Talk title “A TLM Design for Verification Methodology”.

May 2007: Second-place winner of the 3rd TTTC Doctoral Thesis Award Competition at the IEEE VLSI Test Symposium (VTS’07) conference, Berkeley, CA-USA.

April 2007: EDAA grant for attending the PhD Forum at the ACM/IEEE Design, Automation and Test in Europe (DATE’07) conference, Nice, France.

Publications on International Journals:

[J1] F. Busato, N. Bombieri. “A dynamic approach for workload partitioning on GPU architectures”. To appear in IEEE Transactions in Parallel and Distributed Systems, 2016. DOI: 10.1109/TPDS.2016.2631166.

[J2] F.Bistaffa, N. Bombieri, A. Farinelli. “An Efficient Approach for Accelerating Bucket Elimination on GPUs”. To appear in IEEE Transactions on Cybernetics, 2016. DOI: 10.1109-TCYB.2016.2593773.

[J3] N. Bombieri, F. Busato, F. Fummi. “Pro++: A Profiling Framework for Primitive-based GPU Programming”. To appear in IEEE Transactions on Emerging Topics in Computing, 2016. DOI: 10.1109-TETC-2016-2546554.

[J4] V. Bonnici, F. Busato, G. Micale, N. Bombieri, A. Pulvirenti, R. Giugno. “APPAGATO: an APproximate PArallel and stochastic GrAph querying TOol for biological networks”. Bioinformatics, 2016, vol.32(14):2159-66.

[J5] N. Bombieri, D. Drogoudis, G. Gangemi, R. Gillon, M. Grosso, E. Macii, M. Poncino, S. Rinaudo. “Addressing the Smart Systems Design Challenge: The SMAC Platform”. Microprocessors and Microsystems. vol. 39, n.8, 2015, pp. 1158-1173.

[J6] F. Busato, N. Bombieri. “An Efficient Implementation of the Bellman-Ford algorithm for Kepler GPU Architectures”. IEEE Transactions on Parallel and Distributed Systems, vol. 27, n.8, pp. 2222-2233, 2016.

[J7] N. Bombieri, F. Fummi, S. Vinco. “A Methodology to Recover RTL IP Functionality for Automatic Generation of SW Applications”. ACM Transactions on Design Automation of Electronic Systems. vol. 20 n.3, 2015, pp. 1-25, 2015.

[J8] F. Busato, N. Bombieri. “BFS-4K: an Efficient Implementation of BFS for Kepler GPU Architectures”. IEEE Transactions on Parallel and Distributed Systems. vol. 26, n.7, pp. 1826-1838, 2015.

[J9] N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, F. Stefanni, T. Ghasempouri, M. Lora, G. Auditore, M. Negro-Marcigaglia. “Reusing RTL assertion checkers for verification of SystemC TLM models”. Journal of Electronic Testing: Theory and Applications, vol. 31, n.2, 2015, pp. 167-80.

[J10] V. Bonnici, F. Russo, N. Bombieri, A. Pulvirenti, R. Giugno. “Comprehensive reconstruction and visualization of non-coding regulatory networks in human”. Frontiers in Bioengineering and Biotechnology. vol. 69, n. 2, 2014, pp. 1-22.

[J11] N. Bombieri; F. Fummi; V. Guarnieri, G. Pravadelli. “Testbench qualification of SystemC TLM protocols through Mutation Analysis”. IEEE Transactions on Computers. vol. 63, n. 5, 2014, pp. 1248-1261.

[J12] R. Giugno, V. Bonnici, N. Bombieri, A.Pulvirenti, A.Ferro, D. Shasha. “GRAPES: a Software for Parallel Searching on Biological Graphs targeting Multi-core Architectures” PLoS ONE, vol. 8, n. 10, 2013, pp. 1-17.

[J13] N. Bombieri, E.S.M. Ebeid, F. Fummi, M. Lora. “On the Reuse of Heterogeneous IPs into SysML Models for Integration Validation”. Journal of Electronic Testing: Theory and Applications. vol. 29, n.5, 2013, pp. 1-20

[J14] A. Acquaviva, N. Bombieri, F. Fummi, S. Vinco. “Semi-Automatic Generation of Device Drivers for Rapid Embedded Platform Development”. IEEE Transactions on CAD/ICAS. vol. 32, n. 9, 2013, pp. 1293-1306.

[J15] N. Bombieri, F. Fummi, V. Guarnieri. “FAST: An RTL Fault Simulation Framework based on RTL-to-TLM Abstraction”. Journal of Electronic Testing: Theory and Applications. vol. 28, n. 4, 2012, pp. 495-510.

[J16] N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco. “HDTLib: an efficient implementation of SystemC data types for fast simulation at different abstraction levels”. International Journal on Design Automation for Embedded Systems, vol. 16(2), 2012, pp.115-135.

[J17] Guarnieri V. Di Guglielmo G., Bombieri N., Pravadelli G., Fummi, F, Hantson H., Raik J., Jenihhin M., Ubar R. “On the Reuse of TLM Mutation Analysis at RTL”. Journal of Electronic Testing: Theory and Applications, vol. 28, n. 4, 2012 , pp. 435-448.

[J18] N. Bombieri, F. Fummi, G. Pravadelli. “Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions”. IEEE Transactions on Computers. vol. 60, n. 12, 2011, pp. 1730-1743.

[J19] N. Bombieri, M. Ferrari, F. Fummi, G. Di Guglielmo, G. Pravadelli, F. Stefanni, A. Venturelli. “HIFSuite: Tools for HDL Code Conversion and Manipulation «EURASIP Journal on Embedded Systems. vol. 2010 , n. 436328 , 2010 , pp. 1-20.

[J20] N. Bombieri, F. Fummi, D. Quaglia. “System/Network Design Space Exploration based on TLM for Networked Embedded Systems” ACM Transactions on Embedded Computing Systems. vol. 9, n. 4, 2010, pp. 37:1-37:32.

[J21] N. Bombieri, F. Fummi, G. Pravadelli. “Reuse and Optimization of Testbenches and Properties in a TLM-to-RTL Design Flow”. ACM Transactions on Design Automation of Electronic Systems. vol. 13, n. 3, 2008, pp. 47:1-47:22.

[J22] N. Bombieri, A. Fedeli, F. Fummi, G. Pravadelli. “Hybrid Incremental Assertion-Based Verification for Functional Validation in TLM Design Flows”. IEEE Design &Test of Computers. vol. 24, n. 2, 2007, pp. 140-152.

Publications on International Conferences:

[C1] R. Distefano, N. Goncharenko, F.Fummi, R. Giugno, G. Bader, N. Bombieri. “SyQUAL: A platform for qualitative modelling and simulation of biological systems”. In Proc. of IEEE International High-Level Design Validation and Test Workshop (HLDVT), Santa Cruz, CA-USA, October 7-8, 2016, pp.1-8.

[C2] N. Bombieri, F. Busato, F. Fummi, A Fine-grained Performance Model for GPU Architectures. In Proc. of ACM/IEEE Design, Automation and Test in Europe (DATE), Dresden, Germany, 14-18 March, 2016, pp.1-6.

[C3] D. Coati, R. Distefano, N. Bombieri, F. Fummi, M. Mirenda, C. Laudanna, R. Giugno, A SystemC-based Platform for Assertion-based Verification and Mutation Analysis in Systems Biology. In Proc. of IEEE Latin-American Test Symposium (LATS), Foz do Iguacu, Brazil, 6-8 April, 2016, pp. 1-6.

[C4] Bombieri, Nicola; Busato, Federico; Fummi, Franco; Scala, Michele: MIPP: A Microbenchmark Suite for Performance, Power, and Energy Consumption Characterization of GPU architectures. In Proc. of IEEE International Symposium on Industrial Embedded Systems. Krakow (Poland), 23-25 May 2016. pp 1-6.

[C5] S. Aldegheri, J. Barnat, N. Bombieri, F. Busato, M. C˘e˘ska, Milan. Parametric Multi-Step Scheme for GPU-Accelerated Graph Decomposition into Strongly Connected Components. In Proc. of EURO-Par PELGA 2016. Grenoblw (France) 22-26 August. Pp 1-12.

[C6] Bistaffa, Filippo; Bombieri, Nicola; Farinelli, Alessandro: CUBE: A CUDA approach for Bucket Elimination on GPUs. In Proc. of European Conference on Artificial Intelligence (ECAI). The Hague, Hollande, 29 Aug-2 Sept. 2016.

[C7] N. Bombieri, F. Busato; A. Danese; L. Piccolboni; G. Pravadelli, Exploiting GPU Architectures for Dynamic Invariant Mining. In Proceedings of "IEEE International Conference on Computer Design (ICCD)", New York City, NY- USA, October 18-21, 2015, pp. 1-4.

[C8] F. Busato, N. Bombieri. On the Load Balancing Techniques for GPU Applications Based on Prefix-scan. In Proceedings of "IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-15)", Turin, Italy, September, 23-25, 2015, pp. 1-8.

[C9] N. Bombieri, F. Busato, F.Fummi. An Enhanced Profiling Framework for the Analysis and Development of Parallel Primitives for GPUs. In Proceedings of "IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-15)", Turin, Italy, September, 23-25, 2015, pp. 1-8.

[C10] R. Distefano, F. Fummi, C. Laudanna, N. Bombieri, R. Giugno, A SystemC Platform for Signal Transduction Modelling and Simulation in Systems Biology. In Proceedings of "ACM Great lakes symposium on VLSI (GLSVLSI)", Pittsburgh, Pennsylvania, USA, May 20-22, 2015, pp. 1-4.

[C11] N. Bombieri, Riccardo Filippozzi, G. Pravadelli, F. Stefanni, RTL property abstraction for TLM assertion-based verification. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)" , Grenoble (France) , 9-13 March , 2015 , pp. 1-6.

[C12] V. Guarnieri, M. Petricca, A. Sassone, S. Vinco, N. Bombieri, F. Fummi, E. Macii, M. Poncino, A Cross-level Verification Methodology for Digital IPs Augmented with Embedded Timing Monitors. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Dresden, Germany, 24-28 March, 2014, pp. 1-6.

[C13] N. Bombieri, R. Distefano, G. Scardoni, F. Fummi, C. Laudanna, R. Giugno, Dynamic modeling and simulation of leukocyte integrin activation through an electronic design automation framework. In Proceedings of "Conference on Computational Methods in Systems Biology (CMSB)", Manchester, UK, 17-19 November, 2014 , pp. 1-12.

[C14] N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, F. Stefanni, T. Ghasempouri, M. Lora, G. Auditore, M. Negro-Marcigaglia, On the Reuse of RTL assertions in Systemc TLM Verification. In Proceedings of "IEEE Latin-American Test Workshop (LATW)", Fortaleza, Brasil, 12-15 March, 2014, pp. 1-6.

[C15] F. Bistaffa, A. Farinelli, N. Bombieri, Optimising Memory Management for Belief Propagation in Junction Trees using GPGPUs. In Proceedings of "IEEE International Conference on Parallel and Distributed Systems (ICPADS)", Hsinchu, Taiwan, 16-19 December, 2014, pp. 1-8.

[C16] N. Bombieri, H.-Y. Liu, F. Fummi, L. Carloni, A Method to Abstract RTL IP Blocks into C++ Code and Enable High-Level Synthesis. In Proceedings of "ACM/IEEE Design Automation Conference (DAC)", Austin, TX, USA, 2-6 June, 2013, pp. 1-9.

[C17] N. Bombieri, F. Fummi, S. Vinco, On the Automatic Generation of GPU-oriented Software Applications from RTL IPs. In Proceedings of "ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)", Montreal, Canada, Sept 29 - Oct 04, 2013, pp. 1-10.

[C18] N. Bombieri, E.S. Ebeid, F. Fummi, M. Lora, On the reuse of RTL IPs for SysML model generation. In Proceedings of "IEEE International Workshop on Microprocessor Test and Verification (MTV)", Austin, TX, USA, 10–12 December, 2013, pp. 54-59.

[C19] V. Bertacco, D. Chatterjee, N. Bombieri, F. Fummi, S. Vinco, A. M. Kaushik, H. D. Patel, On the Use of GP-GPUs for Accelerating Compute-intensive EDA Applications. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Grenoble, France, 18-22 March, 2013, pp. 1357-1366.

[C20] N. Bombieri, D. Forrini, F. Fummi, M. Laurenzi, S. Vinco, RTL IP abstraction into optimized embedded software. In Proceedings of "IEEE East-West Design & Test Symposium (EWDTS)", Rostov-on-Don (Russia), 27-30 Sept. 2013, 2013, pp. 1-5.

[C21] N. Bombieri, D. Drogoudis, G. Gangemi, R. Gillon, E. Macii, M. Poncino, S. Rinaudo, F. Stefanni, D. Trachanis, M. van Helvoort, SMAC: Smart Systems Co-Design. In Proceedings of "IEEE EUROMICRO DSD/SEAA", Santander, Spain, 4-6 September, 2013, pp. 1-7.

[C22] N. Bombieri, F. Fummi, V. Guarnieri, A. Acquaviva, Energy Aware TLM Platform Simulation via RTL Abstraction. In Proceedings of "IEEE International High Level Design Validation and Test Workshop (HLDVT)", Huntington Beach, CA, USA, 9-10 November, 2012, pp. 156-163.

[C23] N. Bombieri, F. Fummi, V. Guarnieri, FAST-GP: An RTL Functional Verification Framework based on Fault Simulation on GP-GPUs. In Proceedings of "ACM/IEEE Design, Automation and Test in Europe (DATE)", Dresden, Germany, 12-16 March, 2012, pp. 562-565.

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