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Short Biography: I am currently a PostDoc Research Fellow at the Singapore University of Technology and Design (SUTD). My main research activities concern modeling, simulation, and verification of heterogeneous embedded systems. In particular, I focus on the definition of techniques and methodologies for the automatic generation of homogeneous executable models for the efficient simulation of heterogeneous systems. I have expertise on the manipulation of modeling and description languages for HW models. In this field, my main achievement was the definition of a methodology to automatically abstract analog models expressed using Analog Mixed-Signal extensions of HW description languages, and integrate them into homogeneous models of Mixed-Signal devices for efficient simulation.
Since 2015, I started to focus also on the application of formal methods for the design automation and verification of cyber-physical systems. In particular, I focused on the application of Assume-Guarantee Contracts as a formalization for components and requirements within Platform-based design flows. In this field I collaborate with Prof. Pierluigi Nuzzo at the University of Southern California, Prof. Alberto Sangiovanni-Vincentelli at the University of California at Berkeley, and Dr. Yishai Feldman at IBM Research Haifa. The collaboration targets the development of CHASE (Contract-based Heterogeneous Analysis and System Exploration): a contract-based end-to-end requirement engineering framework for system-level design.
Before joining SUTD I was with the Department of Computer Science of the University of Verona (Italy), where I also obtained my Ph.D. in Computer Science in May 2016 supervised by Prof. Franco Fummi. My thesis proposed a unifying platform-based approach for the integration of smart systems from heterogeneous descriptions. While working toward my Ph.D., I spent eight months at the Donald O. Pederson Center of the University of California at Berkeley, where I was supervised by Prof. Alberto Sangiovanni-Vincentelli.
Previously, I received my Master's and Bachelor's degrees from University of Verona, respectively in 2012 and 2010. During my undergraduate studies I spent one year at the University of Linkoping (Sweden) thanks to an Erasmus fellowship. In Linkoping, I had my first research experience, carrying on research on fault-tolerant architectures under the supervision of Prof. Zebo Peng.
So far, I published 4 book chapters, 5 peer-reviewed journal papers and 19 conference papers. Furthermore, I have been actively involved in three European Projects funded by the 7th Framework Programme of the EU, and in different industrial collaborations.

Current position:
Date: 26th March 2018 – current
Position: Postdoctoral Research Fellow,
Institution: Singapore University of Technology and Design,

Previous Positions:
Date: 1st January 2016 – 28th February 2018
Position: Assegnista di Ricerca (PostDoc Fellow),
Institution: Department of Computer Science of the University of Verona (Italy),
Project title: A Virtual Prototyping Environment for Smart Cyber-Physical Systems Design.

Education:
1st January 2013 – 11th May 2016, *Ph.D. in Computer Science*,
Dept. of Computer Science, University of Verona – Italy,
Thesis: *A Unifying Platform-based Approach for the Design of Heterogeneous Systems*,
Advisor: Prof. Franco Fummi.

1st October 2010 – 18th October 2012, *Master's degree in Computer Science and Engineering*,
Dept. of Computer Science, University of Verona – Italy,
Thesis: *SysML as a Unifying Language for Platform-based Design*,
Advisor: Prof. Franco Fummi.

1st October 2005 – 20th October 2010, *Bachelor's degree in Computer Science*,
Faculty of Mathematical, Physical and Natural Sciences, University of Verona – Italy,
Thesis: *Optimization of Assertion Placement in Time-constrained Embedded Systems*,
Advisors: Prof. Graziano Pravadelli, Prof. Zebo Peng.

Visiting Experiences:
Date: October 2016,
Institution: Dept. of Electrical Engineering – University of Southern California,
Supervisor: Prof. Pierluigi Nuzzo,
Visit aimed at finalizing a first demonstrative version of the preliminary synthesis features of CHASE.

Date: January 2015 – September 2015
Institution: Dept. of Electrical Engineering and Computer Science - University of California, Berkeley,
Supervisor: Prof. Alberto Sangiovanni-Vincentelli, (Co-supervisor: Pierluigi Nuzzo)
Period abroad during the Ph.D. program to study Platform-based design with contracts. The ideas behind the development of CHASE have been developed with Pierluigi Nuzzo during these months spent in Berkeley.

Date: January 2009 – December 2009
Institution: Linkoping Institute of Technology, University of Linkoping (Sweden),
Supervisor: Prof. Zebo Peng,
Erasmus fellowship and Research internship at the Embedded System Laboratory.

Teaching Activities:
Position: Contracted Professor of Computer Science,
Institution: Dept. of Electronics, Information and Bioengineering – Polytechnic University of Milan
Program: Bachelor's degree in Mechanical Engineering,
Academic Year: 2017-18.

Position: Contracted Professor of Operating Systems, Laboratory module,
Institution: Dept. of Computer Science - University of Verona,
Program: Bachelor's degree in Computer Science,
Academic Year: 2016-17.

Position: Contracted Professor of Computer Architectures, Exercises module,
Institution: Dept. of Computer Science - University of Verona,
Program: Bachelor's degree in Computer Science,
Academic Years: 2015-16, 2016-17 and 2017-18.

Position: Instructor of Embedded Systems Design, Laboratory module,
Institution: Dept. of Computer Science - University of Verona,
Program: Master's degree in Computer Science and Engineering,
Academic Years: 2013-14, 2014-15, 2015-16, 2016-17 and 2017-18.

Position: Instructor of Design Automation for Embedded Systems, Laboratory module,
Institution: Dept. of Computer Science - University of Verona,
Program: Master's degree in Computer Science and Engineering,
Academic Years: 2014-15, 2016-17 and 2017-18.

Mentoring activities:
Four Master's Students Thesis co-advised.

Four Bachelor's Students Thesis co-advised.
Mentor for five "younger" Ph.D. Students (during the last years of Graduate School and during the Postdoc).

Participation in Funded Projects

Name: Functional mockup Interface extension with support for Discrete Event Languages (FIDEL)
Funding organization and funding programme: University of Verona – Joint Project 2017
Period of the project: February 2017 – January 2019
Role in the project: Coordination of the work package dealing with the automatic generation of Functional Mockup Units from HDL descriptions. Definition of a methodology for the synchronization of multiple discrete-time Functional Mockup Units within a dataflow model.

Name: TOward industrial smart displaYS (TOYS)
Funding organization and funding programme: University of Verona – Joint Project 2016
Period of the project: February 2016 – January 2017
Role in the project: Definition of a methodology for the automatic verification of Industrial Smart Displays.

Name: TerraSwarm Research Center
Funding organizations: DARPA, Semiconductor Research Corporation
Period of the project: January 2013 (Collaboration started in 2016) – 2017
Role in the project: Development of the first prototype of CHASE (https://chase-cps.github.io).

Name: design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties (CONTREX)
Funding organization and funding programme: European Union – Framework Programme 7
Period of the project: October 2013 – September 2016
Role in the project: Research on different Work Packages.

Name: SMArt systems Codesig (SMAC)
Funding organization and funding programme: European Union – Framework Programme 7
Period of the project: October 2011 – March 2015
Role in the project: Research on different Work Packages; development and management of two project demonstrators.

Name and Acronym: Toolchain for next generation Heterogeneous Multicore platforms (TouchMore)
Funding organization and funding programme: European Union – Framework Programme 7
Period of the project: September 2011 – May 2014
Role in the project: Development of an automatic abstraction methodology to automatically produce SysML models from HW description language specifications.

Participation in Industrial Innovation

Company: EXOR International S. p. A., San Giovanni Lupatoto (Verona), Italy
Sector: Industrial automation, Domotics, Internet of Things
Type of collaboration: External consultant, funded project (TOYS joint project) partner
Activities: Definition of a novel verification methodology for the design of the industrial displays.

Organization: Industrial Cyber-Physical Systems Center (iCyPhy) at the University of California, Berkeley
Funding companies: IBM Corporation, United Technology Corporation
Sector: Semiconductors
Type of collaboration: Visiting Research Scholar from January 2015 to September 2015
Activities: Development of a prototypical architectural exploration tool for Cyber-Physical Systems; development of a design flow for the automatic generation of control strategies from requirements for Cyber-Physical Systems.

Company: STMicroelectronics, Agrate Brianza, Italy
Sector: Semiconductors
Type of collaboration: European Project (SMAC, EU FP7) Partnership

Activities: Definition of a novel technique for the virtual prototyping of Micro-electro-mechanical Systems for embedded SW tuning and validation.

Services to the Scientific Community

- **Hands-on Tutorial Chair,**
  ECSI/IEEE Forum on Design and Specification Languages (FDL) 2017
- **Member of the Organizing Committee**
  IEEE International Conference on Electromagnetics in Advanced Applications 2017
- **Member of the Technical Program Committee**
  - Euromicro Conference on Digital Systems Design (DSD) 2016, Special Session on Design of Cyber-Physical Systems,
  - Euromicro Conference on Digital Systems Design (DSD) 2017, Special Session on Design of Cyber-Physical Systems
- **Technical Reviewer** for the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Impact Factor: 1.94)

Publications

Book chapters:

1. S. Vinco, **M. Lora**, and M. Zwolinski. *SystemC-AMS simulation of conservative behavioral descriptions*. In Languages, Design Methods, and Tools for Electronic System Design, pages 151–173, 2016.
2. S. Vinco, **M. Lora**, V. Guarnieri, J. Vanhese, D. Trachanis, and F. Fummi. *Design domains and abstraction levels for effective smart system simulation.* In Smart Systems Integration and Simulation, pages 23–54. Springer, 2016.
3. I. Blanco, …, **M. Lora**, et al. *Smart system case studies. In Smart Systems Integration and Simulation*, pages 195–227. Springer, 2016.
4. F. Fummi, **M. Lora**, F. Stefanni, and S. Vinco. *Code Generation Alternatives to Reduce Heterogeneous Embedded Systems to Homogeneity*. In Languages, Design Methods, and Tools for Electronic System Design, pages 103–124. 2014.

Journal publications:

1. **M. Lora**, S. Vinco, E. Fraccaroli, D. Quaglia, and F. Fummi. *Analog Models Manipulation for Effective Integration in Smart System Virtual Platforms*. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017.
2. **M. Lora**, R. Muradore, D. Quaglia, and F. Fummi. *Simulation alternatives for the verification of networked cyber-physical systems*. Microprocessors and Microsystems, 39(8):843–853, 2015.
3. N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, F. Stefanni, T. Ghasempouri, **M. Lora**, G. Auditore, and M. Marcigaglia. *Reusing RTL assertion checkers for verification of SystemC TLM models*. Journal of Electronic Testing, 31(2):167–180, 2015.
4. N. Bombieri, E. Ebeid, F. Fummi, and **M. Lora**. *On the Reuse of Heterogeneous IPs into SysML Models for Integration Validation*. Journal of electronic testing, Theory and Application (JETTA), 29(5):647–667, 2013.
5. V. Izosimov, G. Di Guglielmo, **M. Lora**, G. Pravadelli, F. Fummi, Z. Peng, and M. Fujita. *Time-constraint-aware optimization of assertions in embedded software*. Journal of electronic testing, Theory and Application (JETTA), 28(4):469–486, 2012.

Conference publications

1. P. Nuzzo, **M. Lora**, Y. Feldman, A. L. Sangiovanni-Vincentelli. "CHASE: Contract-Based Requirement Engineering for Cyber-Physical System Design". In Proc. of ACM/IEEE DATE 2018, pages 1-6.
2. **M. Lora**, S. Centomo, D. Quaglia, F. Fummi. *Automatic Integration of Cycle-accurate Descriptions with Continuous-time Models for Cyber-Physical Virtual Platforms.* In Proc. of ACM/IEEE DATE 2018, pages 1-6.
3. **M. Lora.** *Validation of HMI Applications for Industrial Smart Display.* In Proc. of IEEE HLDVT Workshop 2017, pages 1-8.
4. S. Centomo, **M. Lora**, A. Portaluri, F. Stefanni, F. Fummi, *Automatic Generation of Cycle-Accurate Simulink Blocks from HDL IPs.* In Proc. of ECSI/IEEE FDL 2017, pages 1-8, to appear. Best Paper candidate
5. **M. Lora**, E. Fraccaroli, and F. Fummi. *Virtual prototyping of smart systems through automatic abstraction and mixed-signal scheduling*. In Proc. of ACM/IEEE ASP-DAC 2017, pages 232–237.
6. E. Fraccaroli, **M. Lora**, and F. Fummi. *Automatic abstraction of multi-discipline analog models for efficient functional simulation*. In Proc. of ACM/IEEE DATE 2017, pages 662–665.

7. **M. Lora**, S. Vinco, and F. Fummi. *A unifying flow to ease smart systems integration*. In Proc. of IEEE HLDVT 2016, pages 113–120.2016.
8. E. Fraccaroli, **M. Lora**, F. Fummi, and P. Montuschi. *A fast simulation environment for smart systems validation in presence of electromagnetic interferences.* In Proc of IEEE ICEAA 2016 pp. 740-743.
9. E. Fraccaroli, **M. Lora**, S. Vinco, D. Quaglia, and F. Fummi. *Integration of mixed-signal components into virtual platforms for holistic simulation of smart systems*. In Proc. of the ACM/IEEE DATE 2016, pages 1586–1591.
10. S. Vinco, **M. Lora**, and M. Zwolinski. *Conservative Behavioural Modelling in SystemC-AMS*. In Proc. of ECSI/IEEE FDL 2015, pages 1–8, 2015.
11. **M. Lora**, F. Martinelli, and F. Fummi. *Hardware Synthesis from Software-oriented UML Descriptions.* In Proc. of IEEE 15th International Microprocessor Test and Verification Workshop (MTV). 2014. Pages 1-8.
12. N. Bombieri, F. Fummi, V. Guarnieri, G. Pravadelli, F. Stefanni, T. Ghasempouri, **M. Lora**, G. Auditore, and M. Negro-Marcigaglia. *On the reuse of RTL assertions in SystemC TLM verification*. In Proc. of IEEE LATW, 2015. Pages 1-6.
13. F. Fummi, **M. Lora**, D. Trachanis, J. Van Hese and S. Vinco, Homogeneous simulation: The effective integration solution for smart systems. In *10th IEEE International Conference on Advanced Semiconductor Devices & Microsystems (ASDAM)*, pp. 1-4. 2014.
14. F. Li, E. Dekneuvel, G. Jacquemod, D. Quaglia, **M. Lora**, F. Pecheux, and R. Butaud *"Multi-level modeling of wireless embedded systems*" In Proc of IEEE/ECSI FDL 2014, pages 1-8
15. F. Fummi, **M. Lora**, F. Stefanni, D. Trachanis, J. Vanhese, and S. Vinco. *Moving from Co-Simulation to Simulation for Effective Smart Systems Design*. In Proc. of the ACM/IEEE DATE 2014, pages 1–4, 2014.
16. **M. Lora**, R. Muradore, F. Fummi, and R. Reffato. *Simulation Alternatives for Modeling Networked Cyber-Physical Systems.* In Proc. of Euromicro DSD 2014, pages 1-8.
17. F. Fummi, **M. Lora**, F. Stefanni, and S. Vinco. *Code Generation Alternatives to Reduce Heterogeneous Embedded Systems to Homogeneity*. In Proc of IEEE/ECSI FDL 2014, pages 1-4.
18. N. Bombieri, E. Ebeid, F. Fummi, and **M. Lora**, *On the reuse of RTL IPs for SysML model generation*. In Proc. of IEEE *International Workshop on Microprocessor Test and Verification (MTV) 2012*, pp. 54-59.
19. V. Izosimov, G. Di Guglielmo, **M. Lora**, G. Pravadelli, F. Fummi, Z. Peng, and M. Fujita. *Optimization of assertion placement in time-constrained embedded systems*. In Proc. of IEEE ETS 2011, pages 171–176.

Most significative invited presentations

- *"Automatic Generation of Cycle-Accurate Simulink Blocks from HDL IPs"*, IEEE Forum on specification and Design Languages (FDL) 2017, Verona (Italy), 19th September 2017.
- *"IP-XACT for smart systems design: extensions for the integration of functional and extra-functional models",* IEEE/ECSI Forum on specification and Design Languages (FDL) 2016, Bremen (Germany), 15th September 2016.
- *"Integration of Mixed-signal Components into Virtual Platforms for Holistic Simulation of Smart Systems",* IEEE/ACM Design, Automation And Test in Europe (DATE) 2016, Dresden (Germany), 17th March 2016.
- *"Hardware Synthesis from Software-Oriented UML Descriptions",* 15th International Workshop on Microprocessor Test and Verification 2014, Austin (TX), 16th December 2014.
- "*A Homogeneous Framework for Heterogeneous Cyber-Physical Systems Design",* invited seminar at the Dept. of Computer Science, Columbia University (NY), 12th December 2014.
- Hands-on Tutorial: "*Methods and tools for smart device integration and simulation",* ACM/IEEE Embedded System Week 2014, Greater Noida (India), 12th October 2014.