Curriculum Vitae et Studiorum

Graziano Pravadelli

1. Personal data

Place and date of birth:

Legnago (VR) Italy, 04 July 1974.

Marital status:

Married since July 2003, two sons.

Current position:

Associate professor, Università degli Studi di Verona, Italy, since January 2011.

Co-founder and head of production of EDALab s.r.l. (http://www.edalab.it), since July 2007.

IEEE senior member

Working address:

Dipartimento di Informatica, Università degli Studi di Verona.

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Previous positions:

Assistant professor, Università degli Studi di Verona, Italy, from January 2005 to December 2010.

Post-doc, Università degli Studi di Verona, Italy, from April 2004 to December 2004.

2. National scientific qualifications

National Scientific Qualification for full professor (01/B1) acquired on 19/01/2015.

National Scientific Qualification for full professor (09/H1) acquired on 04/04/2017.

3. Higher education

Ph.D.:

Ph.D., Computer Science, Università degli Studi di Verona, Italy, March 2004. Thesis title: "*Using functional verification to evaluate the accuracy of model checking applied to embedded systems: theory and application*" (advisor: Prof. Franco Fummi).

Laurea:

Laurea degree (summa cum laude), Computer Science, Università degli Studi di Verona, Italy, April 2001. Thesis title (in Italian): "*Simulazione di errore per descrizioni VHDL e SystemC per il test funzionale*" ("*Functional test by fault simulation for VHLD and SystemC models*") (advisor: Prof. Franco Fummi).

4. Awards

Best paper candidate:

A. Danese, F. Filini, G. Pravadelli "A Time-Window Based Approach for Dynamic Assertions Mining on Control Signals", In: IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC). Daejeon, Korea, 5-7 October 2015.

F. Cucchetto, A. Lonardi, G. Pravadelli "*A common architecture for co-simulation of SystemC models in QEMU and OVP virtual platforms*", In: FIP/IEEE International Conference on Very Large Scale Integration (VLSI-SOC). Playa del Carmen, Messico, 6-8 October 2014.

M. Bonato, G. Di Guglielmo, M. Fujita, F. Fummi, G. Pravadelli, "*Dynamic property mining for embedded software"*. In: ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS). Tampere, Finland, 7-12 October 2012, p. 187-196.

N. Bombieri, F. Fummi, G. Pravadelli. *A Mutation Model for the SystemC TLM 2.0 Communication Interfaces.* In: ACM/IEEE Design, Automation and Test in Europe (DATE). Munich, Germany, 10-14 March 2008, p. 396-401.

Selected best paper:

G. Di Guglielmo, F. Fummi, C. Marconcini, G. Pravadelli . F*ATE: a Functional ATPG to Traverse unstabilized EFSMs.* In: IEEE European Test Symposium (ETS). Southampton, UK, 21-24 May 2006. p. 179-184.

5. Scholarships and grants

November 2006: Research grant "Giovani ricercatori 2006", Dipartimento di Informatica, Università degli Studi di Verona, Verona, Italy (1 year).

June 2004: SIGDA grant for presenting the PhD thesis at the "7th SIGDA PhD Forum" co-located with the "41st ACM/IEEE Design Automation Conference (DAC)", San Diego, CA, USA.

January 2002: Research grant "Giovani ricercatori 2001", Dipartimento di Informatica, Università degli studi di Verona, Verona, Italy (1 year)

January 2001: Italian ministry scholarship supporting the PhD course (3 years).

6. Research interests

The research activity of Graziano Pravadelli is related to the following four main fields, partially supported by the research projects reported in Section 9.

1. Modelling and simulation of embedded systems.
2. Semi-formal approaches for embedded system verification.
3. Fault models and test generation for embedded systems.
4. System-level power consumption estimation of embedded systems.

Therefore, research interests of Graziano Pravadelli concern main aspects of the design of embedded systems, including modelling, simulation, verification and testing.

6.1 Modelling and simulation of embedded systems

The ever increasing complexity of modern embedded systems requires that designers consider heterogeneous and often conflicting aspects, such as, for example, the adoption of different levels of abstraction, the integration of digital and analog components, the use of HW dependent software, the awareness of the presence of a physical environment in which the system is embedded, etc. This heterogeneity has been addressed through various modelling and simulation approaches, by adopting both top-down and bottom-up methodologies, and by integrating model-based design, component-based design and co-simulation-based techniques. However, it is evident the lack of a computational model widely accepted that allows integrating heterogeneous components in a homogeneous description that can be easily manipulated and simulated during the various stages of the design flow.

In this context, Graziano Pravadelli coordinated the definition and implementation of a virtual prototyping and modelling environment for embedded systems (HIFSuite – http://www.hifsuite.com) based on the HIF (Heterogeneous Intermediate Format) interchange format, and the definition of the UNIVERcm (Universal Versatile Computational Model) computational model that allows to formalize the semantics of HIF descriptions [5, 36].

Based on HIFSuite, Graziano Pravadelli eventually set up various techniques and methodologies for modelling, integration, simulation and verification of embedded systems [8, 21, 32, 41, 43, 44, 52, 112]. Of particular interest it is the definition of an automatic technique for the abstraction of RTL (Register Transfer Level) models to TLM (Transaction Level Model) models [8], which avoids the co-simulation of mixed-RTL-TLM descriptions that slows down the simulation speed (those RTL), to take full advantage of the greater speed of TLM models.

Most of the activities related to HIFSuite and UNIVERcm were made as part of European projects SYMBAD, VERTIGO, CONTREX, COMPLEX, SMAC and TOUCHMORE for which HIFSuite has become the main tool for the creation of virtual platforms for simulation and verification of complex systems. HIFSuite is currently a commercial product of EDALab.

6.2 Semi-formal approaches for embedded system verification

In the context of verification of embedded systems, the research activities of Graziano Pravadelli focuses on the definition of semi-formal techniques and in particular on the study of approaches for automation and optimization of verification methodologies based on assertions. In this context, the main covered research fields are:

- Assertion-based verification for embedded software [2, 3, 7, 40, 45, 47, 51, 53, 55]. The main contribution of Graziano Pravadelli is represented by having defined a methodology and an automated tool (radCHECK - http://www.verificationsuite.com) to apply assertion-based verification (ABV) to the world of embedded SW. ABV techniques are mainly oriented to check descriptions based on transition systems (e.g., extended finite state machines) typical of the RTL abstraction level, where the time reference for synchronization of models and checkers (simulated components corresponding to the desired assertions) is closely related to the concept of clock cycle. In the context of the embedded software, the absence of such a precise time reference makes it much more difficult to apply ABV techniques. This limitation has been overcome in [4, 45] using the principles of model-based modelling. The research has led the implementation of radCHECK, an automated tool for assertion-based verification of embedded software developed under the VAFER project. radCHECK is currently marketed by STMProducts and developed in collaboration with EDALab with the scientific supervision of Graziano Pravadelli. Other relevant contributions were produced as part of the optimization of assertions in real-time systems, to avoid that the timing constraints imposed by such systems were missed because of the time required for the verification of statements in a context of self-checking [7, 40, 55].
- Automatic generation of assertions [20, 26, 28, 29, 33, 44, 113]. In these works, the traditional flow that involves first defining assertions corresponding to the specifications and then checking them has been reversed. In [28, 33, 44] some methods are presented for automatic extraction of temporal assertions from simulation traces of HW/SW descriptions. Mined assertions can then be compared with the initial specifications to analyse the presence of discrepancies, which would be symptom of an incorrect implementation. Compared to techniques already existing in the literature that extract only Boolean properties, the approaches proposed by Graziano Pravadelli are distinguished by the ability to generate assertions that predicate both at Boolean and non-Boolean domains by extracting arithmetic-logic expression on Boolean, integer and float data types. Extraction of invariants, i.e., arithmetic logic expressions that represent a stable condition

holding on the analysed execution traces, has been investigated too [26, 29] by proposing efficient strategies exploiting the power of GPU architecture for speeding-up the mining phase.

- Reuse and automatic abstraction of assertions [2, 3, 34, 52, 56]. The issues related to the integration and simulation of descriptions represented at different levels of abstraction (e.g., RLT and TLM) and on different domains (e.g., analog, digital) have a great impact in the context of verification too. An assertion initially written for an analog model can not be reused to check the corresponding digital model after its discretization. Similarly, an assertion defined at RTL level need to be rewritten when moving towards the TLM level. In this context, the activity of Graziano Pravadelli was concentrated in the definition of methodologies for the automatic reuse and abstraction of assertions between different domains and abstraction levels in order to avoid costly (in terms of time) and risky (in terms of errors that can be introduced) manuals redefinition. In particular, while there are several works that propose approaches for re-use of assertions from TLM to RTL, the abstraction of assertions from RTL to TLM has been addressed for the first time in [2, 3, 34].
- Assertion qualification [15, 16, 20, 27, 64, 70, 76, 94]. The lack of exhaustiveness is one of the biggest problems related to the use of simulation-based techniques for digital system validation. Formal verification aims at overcoming this problem by proving assertions on mathematical models representing the system implementation. In this context, temporal logic assertions are defined to formally check the correctness of a design implementation with respect to the specification. However, the use of assertions cannot completely assure the correctness of the design implementation. Assertion's vacuity, incompleteness and inconsistency may prevent the effectiveness of assertion-based verification approaches, leading the verification engineers to a false sense of security. To improve the degree of confidence on assertion-based verification, Graziano Pravadelli has proposed several techniques to qualify the set of assertions in terms of design coverage [15, 16, 70, 94], vacuity analysis [64, 76] and degree of interestingness [27], when used for checking the correctness of a model. The work of Pravadelli distinguishes from previous approaches since it is based on mutant analysis rather than symbolic methods, which guarantees a more accurate estimation of assertion quality in a shorter time.

Most of the activities related to the semi-formal-verification of embedded systems have been undertaken under the projects EFFORT, VAFER, OPTIMUM and SMAC and collaborations between EDALab and the University of Verona.

6.3 Fault models and test generation for embedded systems

Automatic test pattern generation is the basis of all the verification techniques that are based on simulation. Very often this generation is driven by metrics that require the application of fault models to simulate the presence of errors (design) or defects (physical) within the model and/or its implementation. Such metrics measure the quality of the generated sequences according to their ability to "find" faults injected by comparing the results of the fault-free model/implementation with those of the

models/implementations perturbed by faults. In this context, Graziano Pravadelli has proposed numerous techniques for the generation of test sequences integrating symbolic, concolic and concrete approaches [9, 24, 50]. In addition, Graziano Pravadelli defined a language for specifying test sequences (Testbench Specification Language) [42, 34] particularly suitable to represent constraints that must be met to activate (and then test) special conditions that would not be analysed by using traditional probabilistic approaches and that would require too space-time consuming resources for an exhaustive evaluation.

Graziano Pravadelli worked also on fault modelling strategies [1, 6, 3, 22, 38, 43, 54], both for hardware descriptions and embedded software. In particular, it is worth noting the work published in [9] where for the first time a fault model for TLM description is proposed.

Most of the activities related to the semi-formal-verification of embedded systems were carried on as part of the VAFER and OPTIMUM projects and collaborations between EDALab and the University of Verona.

6.4 System-level power consumption estimation of embedded systems

Recently, Graziano Pravadelli has moved his attention also towards system-level modeling of extra-functional properties, targeting, in particular, power behaviors of digital IPs. In this field he proposed an innovative approach for the automatic generation of power state machines (PSMs) that allow validating the power consumption of a system inside a virtual prototype [25]. Currently, none other approach exists in the literature that automatically generate PSMs. The approach starts by dynamically mining temporal assertions from the functional traces. From them, the states and the transitions of a corresponding set of PSMs are generated and optimized by exploiting a calibration process relying on a set of training power traces. Future research activities in this context will be devoted to address the generation of PSMs for time-dependent and data dependent designs and their abstraction towards the TLM level.

7. Transfer of technology

Graziano Pravadelli is co-founder and head of the production of EDALab s.r.l. (http://www.edalab.it), an Italian SME whose mission consists of giving support for innovation and technology transfer in embedded system modeling and verification. EDALab was founded on July 16, 2007 and it currently employs 13 persons in the development of embedded SW, and the design of CAD tools for modelling and verification of networked embedded systems. EDALab has been involved in several industrial and scientific projects (including the EU projects CONTREX, COMPLEX, SMAC and COCONUT) in cooperation with international companies (e.g., STMicroelectronics, Keysight (Agilent), Exor International), universities and research centres.

Among EDALab's main products, HIFSuite and radCHECK found their scientific basis on the research activity of Graziano Pravadelli.

8. Teaching activities and teaching books

Graziano Pravadelli's teaching activities include:

- Teaching activity at Università degli Studi di Verona, Italy (since 01/2005):
    - operating systems (more than 800 hours);
    - advanced operating systems (more than 600 hours);
    - design automation of embedded systems (more than 200 hours),
    - basic information technology (more than 150 hours).
- Teaching activity at Politecnico di Milano, Italy (since 09/2002):
    - basic informatics (more than 1000 hours).
- Teaching activity at University of Trento, Italy (since 02/2015):
    - operating systems (120 hours).

Graziano Pravadelli is co-author of the book chapter (in Italian):

- D. Botturi, F. Fontana, G. Pravadelli, "Appendice A: Laboratorio di Linux", in V. Manca *"Metodi Informazionali"*, Bollati Boringhieri 2003, pp. 129-206.

Graziano Pravadelli translated from English to Italian with Prof. Alfredo Petrosino the book:

- D.M. Dhamdhere, "*Operating systems. A concept based approach*", McGraw-Hill, 2008.

Graziano Pravadelli translated from English to Italian the book:

- D.M. Dhamdhere, "*A Solutions Manual for Operating systems. A concept based approach*", McGraw-Hill, 2008.

Graziano Pravadelli translated from English to Italian the following book chapters:

- "Istruzioni Macchina IA-32", in C. Hamacher, Z. Vranesic, S. Zacky *"Introduzione all'architettura dei calcolatori"*, *McGraw-Hill* 2007, pp. 291-340.
- "Elenco delle Istruzioni Macchina IA-32", in C. Hamacher, Z. Vranesic, S. Zacky *"Introduzione all'architettura dei calcolatori"*, *McGraw-Hill* 2007, pp. 633-656.

Graziano Pravadelli revised the following books:

- D.M. Dhamdhere, "*Operating systems. A concept based approach*", McGraw-Hill Intenational Edition 2003.
- A. Bellini, A. Guidi, "*Linguaggio C - Guida alla programmazione*", McGraw-Hill 2006.

9. Advising activities

Graziano Pravadelli's advising activities include:

- Advising of 3 PhD students at Università degli Studi di Verona, Italy
    - Tara Ghasempouri, *"Improving ABV by automatic generation and abstraction of PSL assertions"*. Graduation date: May 2016

  - Alessandro Danese, *"System-level functional and extra-functional characterization of SoCs through assertion mining"*. Expected graduation date: May 2018
  - Florenc Demrozi, "*IoT for ambient assisted living*". Expected graduation date: May 2020

- Co-advising of 6 PhD students at Università degli Studi di Verona, Italy:
  - Valerio Guarnieri, *"Design and verification techniques for TLM-based design flows"*, May 2013.
  - Sara Vinco, *"Reuse and integration of heterogeneous components for efficient embedded software generation"*, May 2013.
  - Luigi Di Guglielmo, *"Realizability of embedded controllers: from hybrid models to concrete implementations"*, May 2012.
  - Giuseppe Di Guglielmo, *"On the validation of embedded systems through functional ATPG"*, April 2009.
  - Nicola Bombieri, *"A TLM design for verification methodology"*, March 2008.
  - Cristina Marconcini, *"A Functional ATPG as a bridge between validation and testing"*. March 2008.
- Advising of 12 research fellows (including 2 post-doc students).
- Advising of more than 70 between undergraduate and graduate student thesis in the field of embedded systems and operating systems at Università degli Studi di Verona, Italy.

10. Organizational activities

Graziano Pravadelli has participated to organizational activities in the context of:

- national and international projects;
- review activities and programme committee;
- institutional activities.

10.1 Funded European projects with peer review

Graziano Pravadelli has participated to the research activities in the following projects European projects:

1. Title: Design of embedded mixed-criticality control systems under consideration of extra-functional properties (CONTREX FP7-ICT-2013-10-611146)
   Funding organization: European commission
   Funding schema: Large-scale integrating project
   Period: October 2013 – September 2016
   Number of participants: 15
   Achieved contribution: € 241520

Role in the project: project leader of "system analysis, validation and exploration" of EDALab research unit and project manager of HIFSuite development.

2. Title: Smart system co-design (SMAC FP7-ICT-2011-7-288827)
   Funding organization: European commission
   Funding schema: Large-scale integrating project
   Period: October 2011 – March 2015
   Number of participants: 17
   Achieved contribution: € 473096
   Role in the project: project leader of work package 2 concerning the "co-simulation platform" for EDALab research unit and project manager of HIFSuite development.
3. Title: Automatic Customizable Tool-chain for Heterogeneous Multicore Platform Software Development (TOUCHMORE FP7-ICT-2011-7-288166)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: September 2011 – September 2014
   Number of participants: 8
   Achieved contribution: € 300000
   Role in the project: project manager of HIFSuite development.
4. Title: Codesign and power management in platform-based design space exploration (COMPLEX FP7-ICT-4-247999)
   Funding organization: European commission
   Funding schema: Large-scale integrating project
   Period: December 2009 – November 2012
   Number of participants: 15
   Achieved contribution: € 240000
   Role in the project: project manager of HIFSuite development.
5. Title: A correct by construction workbench for design and verification of embedded systems (COCONUT FP7-2007-IST-1-217069)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: January 2008 - June 2010
   Number of participants: 10
   Achieved contribution: € 340000
   Role in the project: discrete system project manager.
6. Title: Verification and validation of embedded design workbench (VERTIGO IST-2006-033709)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project

Period: June 2006 - November 2008

Number of participants: 7

Achieved contribution: € 346000

Role in the project: technical responsible of the research unit.

7. Title: Formal verification in system level based design (SYMBAD IST-2001-34607)
   Funding organization: European commission
   Funding schema: Small or medium scale focused research project
   Period: March 2002 - October 2004
   Number of participants: 4
   Achieved contribution: € 290000
   Role in the project: coordinator of the development of the research unit applications.

10.2 Funded National projects with peer review

1. Title: Modeling and simulation of complex integrated systems for multimedia applications (CNR01)
   Funding organization: National research center (CNR)
   Funding schema: research project
   Period: October 2001 – September 2002
   Number of participants: 4
   Achieved contribution: € 40000
   Role in the project: Coordinator of the development of research unit applications.
2. Title: Modeling, simulation and validation of system on chips (PRIN02)
   Funding organization: Italian Research Ministry (MIUR)
   Funding schema: National interest research project (PRIN)
   Period: May 2002 – April 2004
   Number of participants: 6
   Achieved contribution: € 52000
   Role in the project: Coordinator of the development of research unit applications.
3. Title: Reuse of IP-core in distributed embedded systems (RISE)
   Funding organization: Università degli Studi di Verona
   Funding schema: Young researchers 2001
   Period: January 2002 – December 2002
   Number of participants: 1
   Achieved contribution: € 5900
   Role in the project: scientific coordinator.
4. Title: Modeling, simulation and verification of MPSoC platforms (PRIN05)
   Funding organization: Italian Research Ministry (MIUR)
   Funding schema: National interest research project (PRIN)

Period: January 2006 – December 2008
Number of participants: 5
Achieved contribution: € 41000
Role in the project: technical manager of the research unit.

5. Title: A smooth refinement flow for co-designing of hardware/software threads (SOFT)
   Funding organization: Università degli Studi di Verona
   Funding schema: Young researchers 2006
   Period: January 2007 – December 2007
   Number of participants: 1
   Achieved contribution: €2500
   Role in the project: scientific coordinator.
6. Title: Yield Improvement in Nanotechnology Production Process of Standard Cells Based Integrated Circuits (ImpNanoIC)
   Funding organization: PDF Solutions, Desenzano del Garda (BS)
   Funding schema: Joint project 2005, Università di Verona
   Period: January 2007 – December 2007
   Number of participants: 2
   Achieved contribution: € 51000
   Role in the project: technical project manager.
7. Title: An EFSM-based Framework for Designing and Verifying Embedded Software (EFFORT)
   Funding organization: STM Products, Verona
   Funding schema: Joint project 2007 Università di Verona
   Period: January 2008 – December 2009
   Number of participants: 2
   Achieved contribution: € 142000
   Role in the project: technical project manager.
8. Title: Optimizing dependability via mutation analysis for microelectronics (OPTIMUM)
   Funding organization: STM Products, Verona
   Funding schema: Joint project 2010 Università di Verona
   Period: January 2011 – December 2012
   Number of participants: 2
   Achieved contribution: € 85500
   Role in the project: project manager.
9. Title: Formal verification of embedded Systems (VAFER)
   Funding organization: Regione Veneto.
   Funding schema: Regional project to support industrial research activity, experimental

analysis, innovation and technological dissemination (L.R. n.9 18/05/2007)
Period: October 2010 – September 2012
Number of participants: 4
Achieved contribution: € 183000
Role in the project: scientific coordinator.

10. Title: Smart pole WSN network (SPAWNE)
    Funding organization: Telefin s.p.a (VR)
    Funding schema: Joint project 2014, Università di Verona
    Period: January 2015 – December 2015
    Number of participants: 2
    Achieved contribution: € 31220
    Role in the project: scientific coordinator.

10.3 Industrial projects

1. Title: Application of an hybrid methodology for functional verification based on formal techniques and test pattern generation (STM01)
   Funding organization: STMicroelectronics – Agrate Brianza
   Funding schema: industrial project
   Period: May 2001 – April 2002
   Number of participants: 2
   Achieved contribution: € 25000
   Role in the project: Coordinator of the development of applications.
2. Title: Development of an automatic system for the validation of a development environment of embedded SW
   Funding organization: STM Products, Verona
   Funding schema: Industrial project
   Period: April 2009 – December 2009
   Number of participants: 2
   Achieved contribution: € 70000
   Role in the project: technical manager.
3. Title: Localization of Visual Studio 2012 MSDN Library
   Funding organization: Microsoft Corp. Redmond USA
   Period: October 2013 – April 2014
   Number of participants: 2
   Achieved contribution: € 10000
   Role in the project: coordinator
4. Title: Localization of Visual Studio 2012 MSDN Library
   Funding organization: Microsoft Corp. Redmond USA

Period: June 2012 – September 2012
Number of participants: 2
Achieved contribution: € 15000
Role in the project: coordinator

5. Title: An innovative system for monitoring and control based on wireless sensors
   Funding organization: ABS Computers, Verona
   Period: January 2012 – December 2012
   Number of participants: 2
   Achieved contribution: € 30000
   Role in the project: coordinator

10.4 Participation in programme committees and referee activities

Graziano Pravadelli has been selected by the steering committees to serve as:

- Local chair of the ECSI Forum on Specification and Design Languages (FDL) 2017;
- General chair of the IFIP/IEEE International Conference in Very Large Scale Integration (VLSI-SoC) 2018.
- Finance chair of the ACM/IEEE International Symposium on Networks-on-Chip (NOCS) 2014.

Graziano Pravadelli has been member of the programme committee of the following international conferences:

- ACM/IEEE Design Automation and Test in Europe (DATE) since 2016 (track chair of system simulation and validation in 2017);
- ECSI Forum on Specification and Design Languages (FDL) since 2016 (track chair of Tools and Techniques);
- ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) since 2011;
- IFIP/IEEE International Conference in Very Large Scale Integration (VLSI-SoC) since 2010 (track chair of Prototyping, Verification, Modeling, and Simulation since 2015);
- International Conference on VLSI Design (VLSID) in 2017;
- IEEE Biennial Baltic Electronics Conference (BEC) since 2008;
- Design, Analysis and Tools for Integrated Circuits and Systems (DATICS) from 2008 to 2012;
- International Conference on Information and Software Technologies from 2014 to 2016.

Graziano Pravadelli has been organizer and speaker of the following tutorials:

- Methods and tools for smart device integration and simulation
  In ACM/IEEE Embedded Systems Week (ESWEEK) 2014, New Delhi, India
- Assertion-based verification: a Common Verification Infrastructure for SoC and Embedded Software.
  In ACM/IEEE Design, Automation and Test in Europe (DATE) 2013, Grenoble, France.

- Assertion-based verification for SoC and embedded software.
  In IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) 2012, Sydney, Australia.

Graziano Pravadelli has cooperated as reviewer for:

- several international conferences: IEEE CODES+ISSS, ACM/IEEE DAC, ACM/IEEE DATE, IEEE ETS, ACM GLSVLSI, IEEE HLDVT, IEEE ITC, IEEE MEMOCODE, IEEE MTV, IEEE BEC, IEEE FDL, IEEE ICCAD, IFIP/IEEE VLSI-SOC, and
- several international journals: ACM Transactions on Design Automation of Electronic Systems, ACM Transactions on Embedded Computing, IEEE Transaction on Computers, IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Kluwer International Journal of Parallel Programming, Springer Design Automation for Embedded Systems, Springer Journal of Electronic Testing, Elsevier Microprocessors and Microsystems, Eurasip Journal of Embedded Systems, IEEE Eletronic Notes, Elsevier Integration, The VLSI Journal).

Graziano Pravadelli has served as referee for the evaluation of the research of Italian Universities and Research Centres (VQR 2011-2014).

10.5 Institutional activity concerning quality assurance

Graziano Pravadelli has served at University of Verona in the following roles:

- Member of the Quality Assurance Board (Presidio per l'Assicurazione della Qualità), since March 2016.
- President of the self-evaluation commission and responsible for AVA (Autovalutazione, Valutazione periodica, Accreditamento) of the master course on Computer Science and Engineering (from 2014 to February 2016), in charge of managing the quality assurance procedures in accordance with the AVA system introduced with the Italian Law 20/12/10 n. 240.
- President of the self-evaluation commission and AVA responsible of the bachelor course on Computer Science (from 2011 to 2014), in charge of managing the quality assurance procedures in accordance with the AVA system introduced with the Italian Law 20/12/10 n. 240.
- President of the self-evaluation commission of the bachelor course on Computer Science (from 2009 to 2010), in charge of managing the quality assurance procedures and the redaction of the *Rapporto di Autovalutazione* (RAV).

Since July 2015, Graziano Pravadelli is part of the Albo "Esperti della Valutazione – Profilo Esperti Disciplinari" of the Italian National Agency for the Evaluation of Universities and Research Institute (ANVUR) for the 09 Area.

10.6 Other institutional activity

Graziano Pravadelli has serviced at University of Verona in the following roles:

- President of the Comitato Area CIVR 09 (from 2008 to 2010).

- Delegate of the Teaching Staff Council for the post-graduate degree in Computer Science at the Graduate School of Science Engineering Medicine (from 2007 to 2009).

11. Publications

11.1 International journals

1. D. Ferraretto, G. Pravadelli, Simulation-based fault injection with QEMU for speeding-up dependability analysis of embedded software, «Journal of Electronic Testing: Theory and Applications», vol 32, n.1, 2016, pp. 43-57.
2. N. Bombieri, F. Fummi V. Guarnieri, G. Pravadelli F. Stefanni; T. Ghasempouri, M Lora, G. Auditore, M. Negro Marcigaglia, Reusing RTL assertion checkers for verification of SystemC TLM models, «Journal of Electronic Testing: Theory and Applications» , Vol. 31, n.2, 2015 , pp. 167-180.
3. N. Bombieri, F. Fummi, V. Guarnieri. G. Pravadelli, Testbench qualification of SystemC TLM protocols through Mutation Analysis. «IEEE Transactions on Computers». Vol. 63, n.5, 2014, pp. 1248-1261.
4. G. Di Guglielmo, L. Di Guglielmo, A. Foltinek, M. Fujita, F. Fummi, C. Marconcini, G. Pravadelli. On the integration of model-driven design and dynamic assertion-based verification for embedded software. «The Journal of Systems and Software» , vol. 86 , 2013 , pp. 2013-2033.
5. L. Di Guglielmo, F. Fummi, G. Pravadelli, F. Stefanni, S. Vinco. UNIVERCM: The UNIversal VERsatile Computational Model for Heterogeneous System Integration. «IEEE Transactions on Computers» , vol. 62 , 2013 , pp. 225-241.
6. V. Guarnieri, G. Di Guglielmo, N. Bombieri, G. Pravadelli, F. Fummi, H. Hantson, J. Raik, M. Jenihhin, R. Ubar. On the Reuse of TLM Mutation Analysis at RTL. «Journal of Electronic Testing: Theory and Applications», vol. 28 , n. 4 , 2012 , pp. 435-448.
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Verona, July 8, 2017

Graziano Pravadelli

DICHIARAZIONE SOSTITUTIVA DI CERTIFICAZIONE e/o SOSTITUTIVA DELL'ATTO DI NOTORIETA' (Art. 19, 46 e 47 D.P.R. n. 445 del 28/12/2000)

Il sottoscritto Graziano Pravadelli nato a Legnago (VR) il 04/07/1974, residente in Legnago (VR) via Ospital Vecchio 32, tel. 3204212799, C.F. PRVGZN74L04E512Z

consapevole della responsabilità penale cui può andare incontro in caso di dichiarazione mendace, ai sensi dell'art. 76 del D.P.R. 445 del 28/12/2000,

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- di possedere tutti i titoli riportati nel presente curriculum e la veridicità di quanto in esso dichiarato;
- che l'apporto di ciascun autore nelle pubblicazioni elencate nella sezione 11 del presente curriculum è da ritenersi paritetico;
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Verona, 08/07/2017

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