



Asynchronous Design Seminar at University of Verona – Lecture Notes 6

Asynchronous Control Circuits – PTnet to MSFSM
Decomposition Flow

State Explosion Revisited

Concurrent Specification

State Space

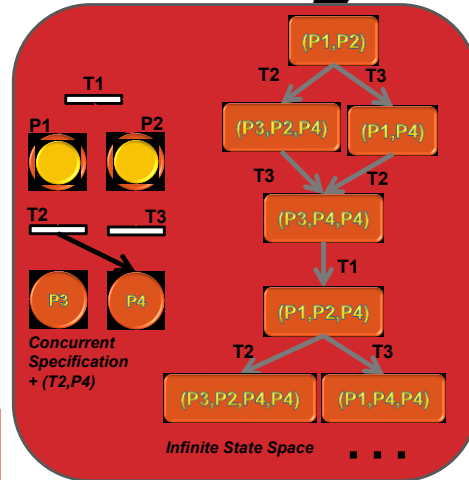
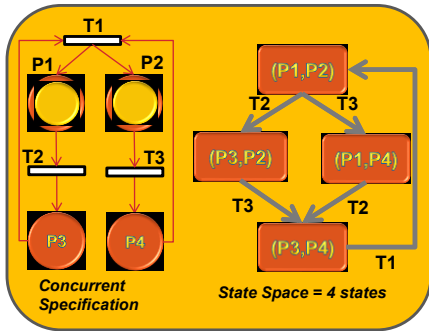
Implementation

- *Logic Synthesis and Verification require specification's full state space*
- *State space size is exponential compared to the specification*

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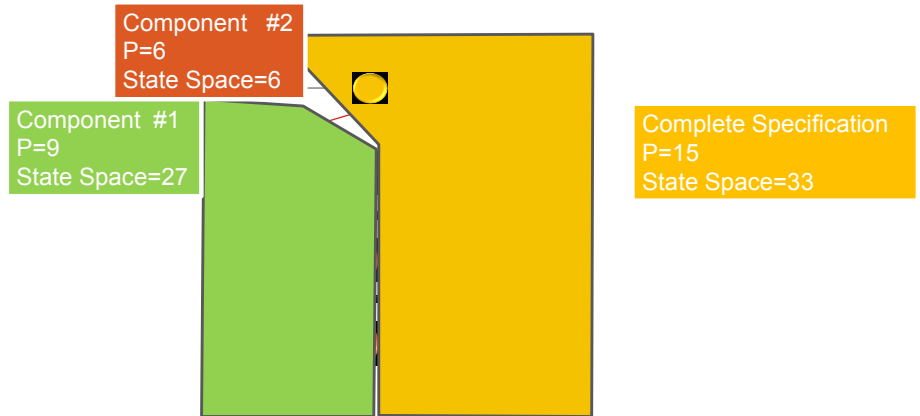
Specification and Confluence



• Changes at the Concurrent Specification Level Have Unpredictable Results at the State Space

▶ 3

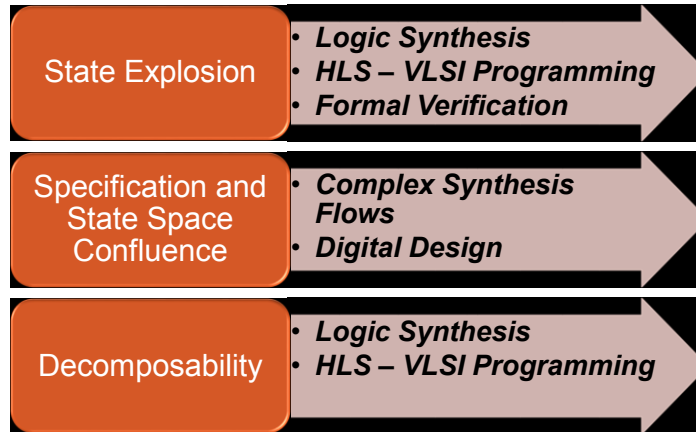
PTnet Decomposability



• Concurrent Specification Decomposition is Unpredictable as it is Evaluated with Specification Metrics, e.g. number of places.

▶ 4

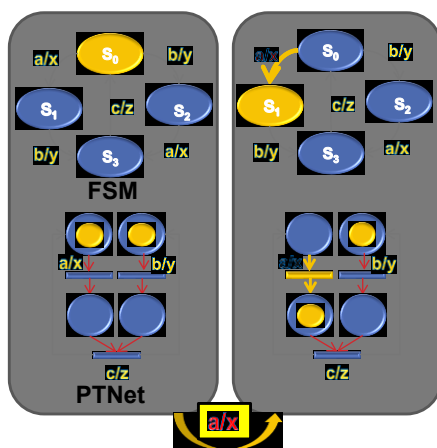
Applications



▶ 5

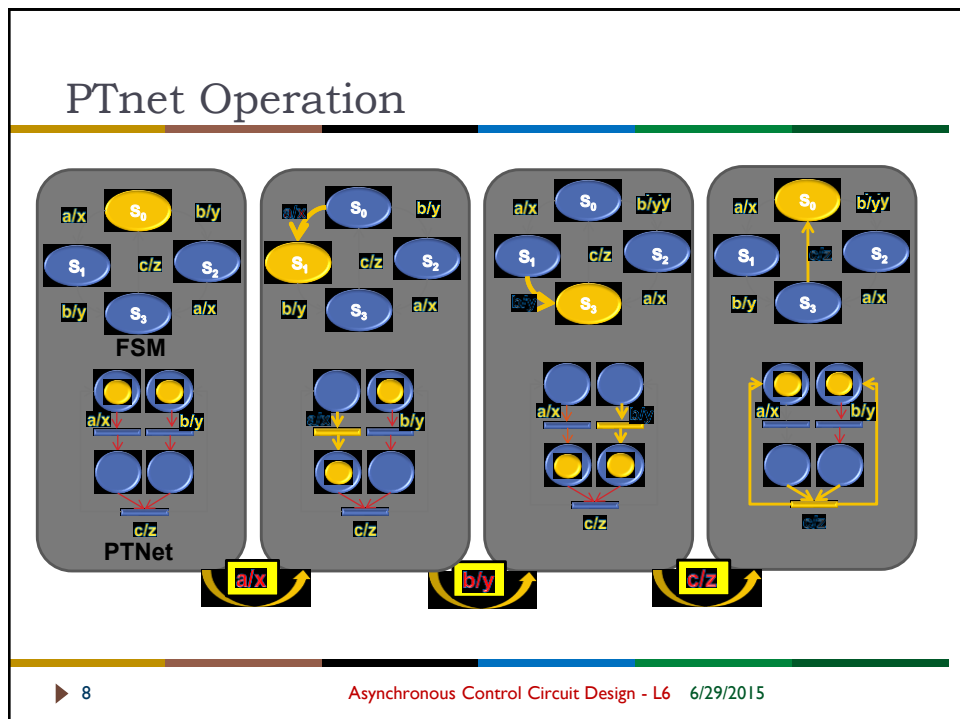
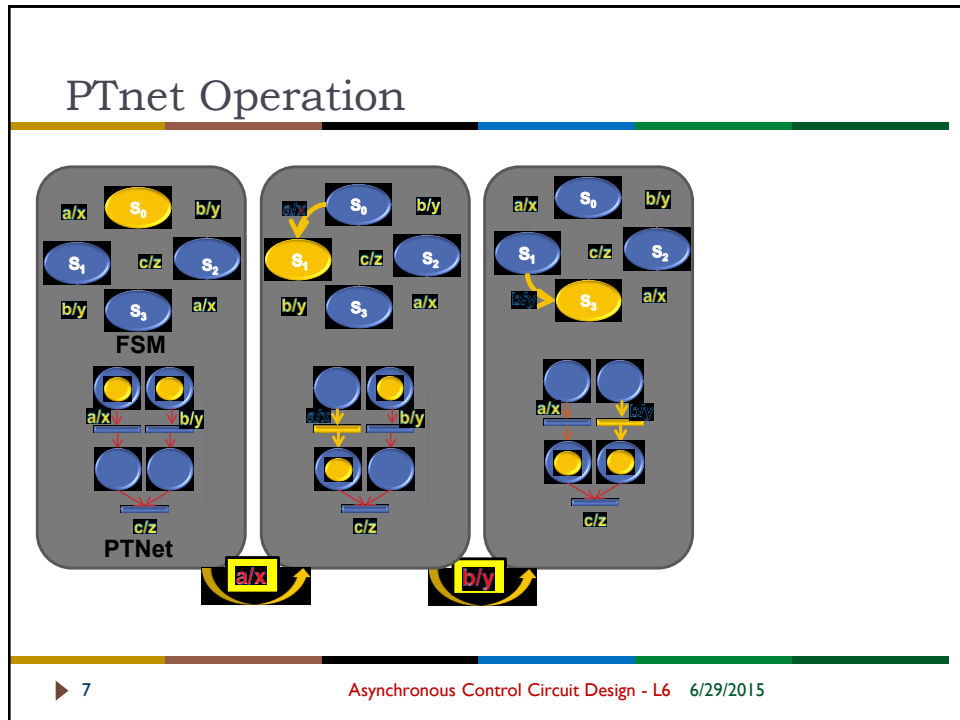
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PTnet Operation




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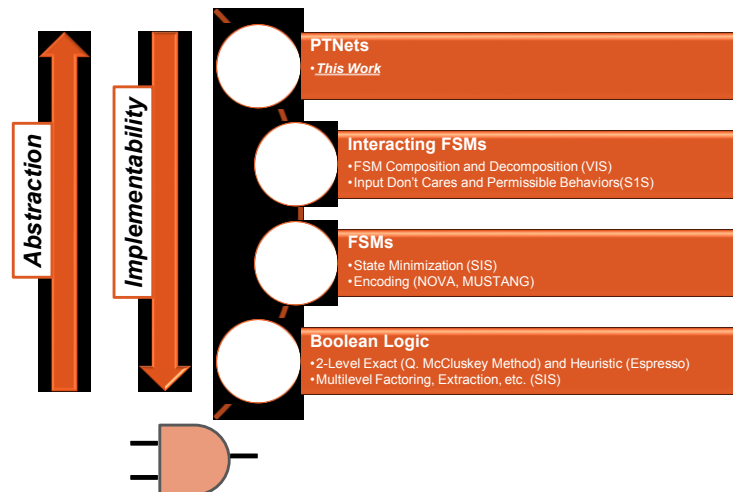
Taxonomy of Control Model Expressiveness

Algebra	FSM		Inter. FSMs	PTNet
$S_0 = S_1.b + S_2.a + S_0.(a+b)'$ $S_1 = S_0.a + S_1.b'$ $S_2 = S_0.b + S_2.a'$ $x = S_0.a + S_1 + S_2.a$				
Control Model	State Space	Choice	Concurrency	Synchronization
<i>Algebra</i>	Implicit	Implicit	Implicit	Implicit
<i>FSM</i>	Explicit	Explicit	Implicit	Implicit
<i>Inter. FSMs</i>	Implicit	Explicit	Explicit	Implicit
<i>PTNet</i>	Implicit	Explicit	Explicit	Explicit

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Synchronous Control Model Implementation



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Asynchronous Control Model Implementation

(A,BM)FSM Synthesis ¹	PTNet Synthesis ²	Decomposition ⁴	Structural Synthesis ⁵	Direct Mapping ³
<ul style="list-style-type: none"> Conventional FSM Heuristics Exponential Concurrent Specifications 	<ul style="list-style-type: none"> Compact Concurrent Specifications Exponential Synthesis Time 	<ul style="list-style-type: none"> Lower Synthesis Time Infeasible Implementation Worst Case Exponential 	<ul style="list-style-type: none"> Lower Synthesis Time Worst Case Exponential 	<ul style="list-style-type: none"> Linear Synthesis Time Suboptimal Results

¹K. Y. Yun and D. L. Dill, "Automatic synthesis of extended burst-mode circuits", IEEE TCAD, 1999

²J. Cortadella et al., "Logic Synthesis of Asynchronous Controllers and Interfaces", Springer-Verlag, 2002.

³D. Sokolov et al., "Direct Mapping of Low-Latency Asynchronous Controllers from STGs", IEEE TCAD, 2007

⁴D. Wist et al., "Signal transition graph decomposition: internal communication for speed independent circuit implementation", IET Computers & Digital Techniques, 2011

⁵E. Pastor et al. "Structural Methods for the Synthesis of Speed-Independent Circuits", IEEE TCAD, 1998



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Commonly used PTnet Implementation Flows

Direct Mapping*

- Linear Complexity
- Suboptimal Result

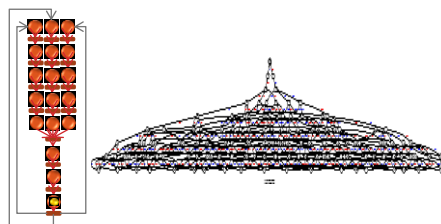


^{D.} Sokolov, A. V. Bystrov, and A. Yakovlev, "Direct Mapping of Low-Latency Asynchronous Controllers from STGs," IEEE TCAD, 2007.

[#]J. Cortadella et al., Logic Synthesis of Asynchronous Controllers and Interfaces. Springer-Verlag, 2002.

Synthesis[#]

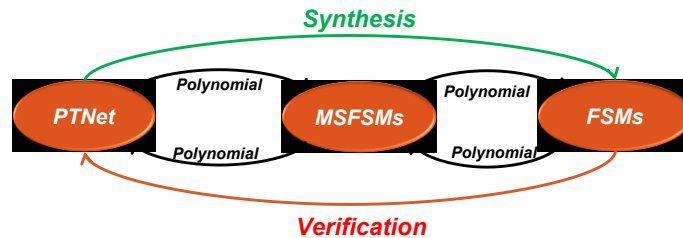
- Globally Optimal Result
- Exponential Complexity



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Multiple Synchronised FSMs (MSFSMs) Model

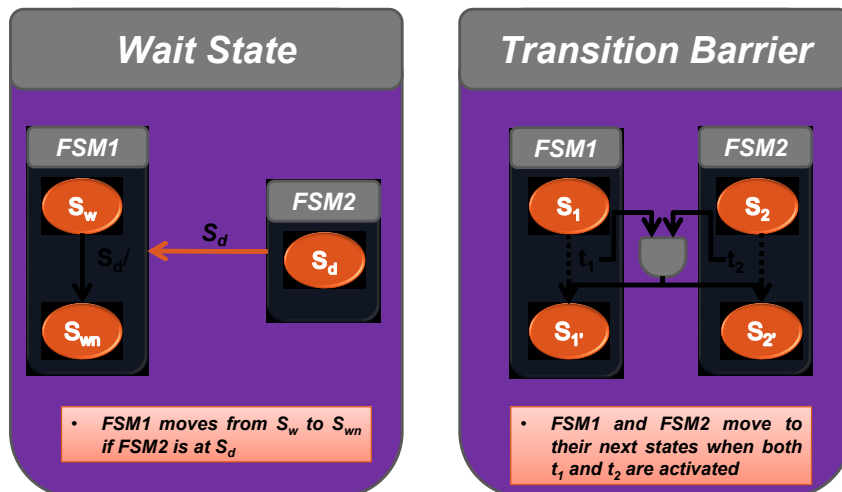
- ▶ Novel Model for Concurrent Control Specifications
 - ▶ Parallel Tasks Described with FSMs
 - ▶ Synchronization explicitly described based on two primitives
 - ▶ **Transition Barriers, Wait States**
 - ▶ Polynomial Synthesis and Verification Paths



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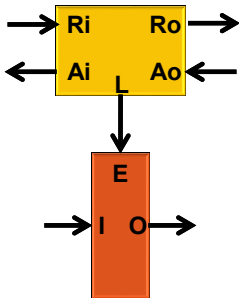
MSFSM Synchronisation Primitives



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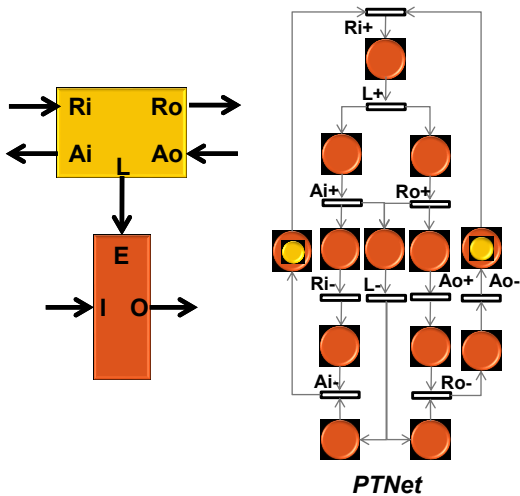
MSFSMs Example – 4-phase Latch Controller



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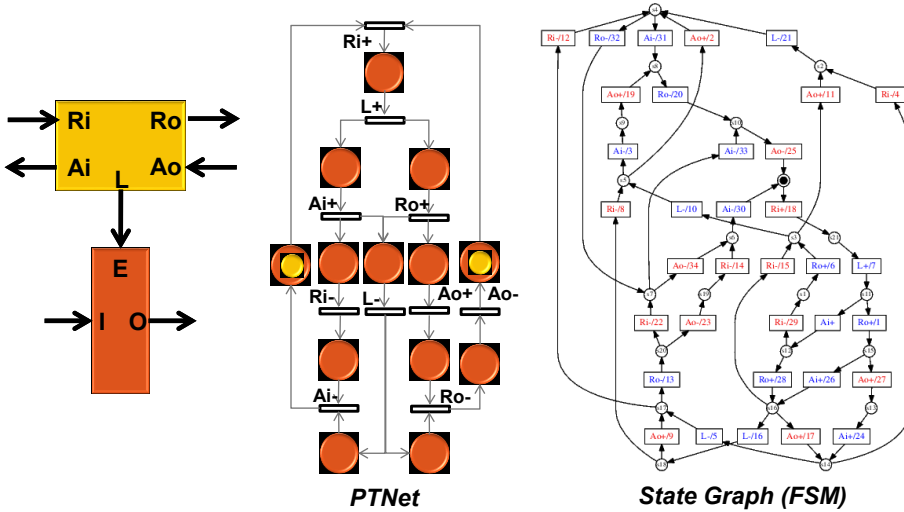
MSFSMs Example – 4-phase Latch Controller



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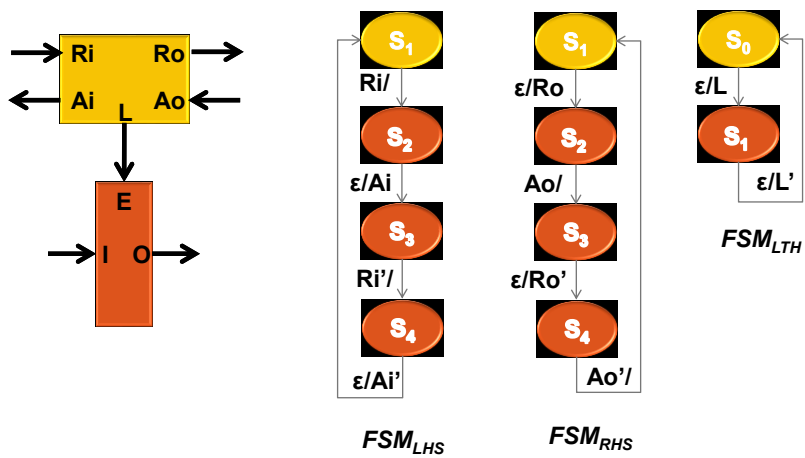
MSFSMs Example – 4-phase Latch Controller



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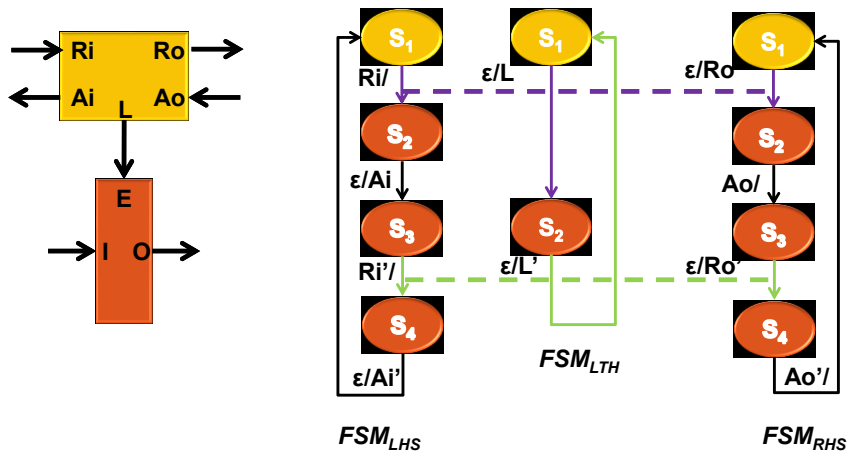
MSFSMs Example – 4-phase Latch Controller



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MSFSMs Example – 4-phase Latch Controller



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Synchronous Synthesis Flow

PTNet Synthesis Flow to Synchronous Circuit

PTNet Decomposition to FSMs

FSMs Synchronization

PTNet Decomposition to S-Components

S-Components Transformation to FSMs

Synchronization Primitives Extraction

Synchronization Integration

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PTnet to S-Component Decomposition

▶ Step 1/4

PTNet

SC₁

PTNet to S-Component Decomposition

S-Component to FSM Mapping

Synchronization Primitive Extraction

Synchronization Integration

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PTnet to S-Component Decomposition

▶ Step 1/4

PTNet

SC₁

SC₂

PTNet to S-Component Decomposition

S-Component to FSM Mapping

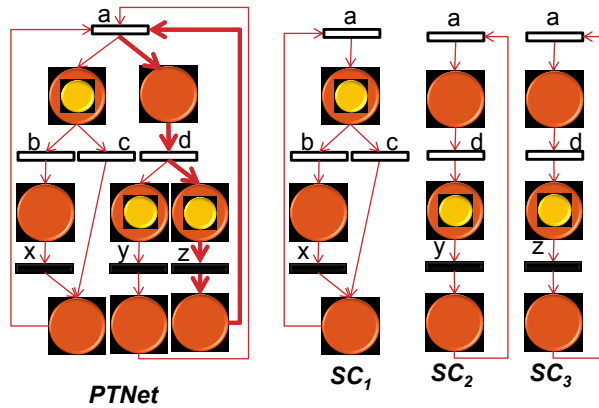
Synchronization Primitive Extraction

Synchronization Integration

▶ 22
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PTnet to S-Component Decomposition

▶ Step 1/4



PTNet to S-Component Decomposition

S-Component to FSM Mapping

Synchronization Primitive Extraction

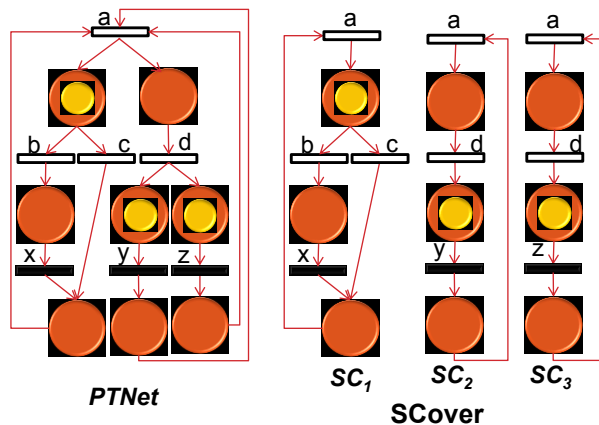
Synchronization Integration

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PTnet to S-Component Decomposition

▶ Step 1/4



PTNet to S-Component Decomposition

S-Component to FSM Mapping

Synchronization Primitive Extraction

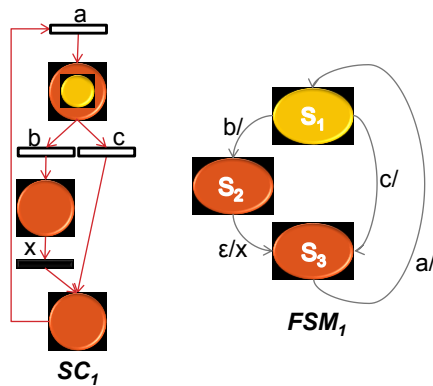
Synchronization Integration

▶ 24

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S-Component to FSM Mapping

► Step 2/4



PTNet to S-Component Decomposition

S-Component to FSM Mapping

Synchronization Primitive Extraction

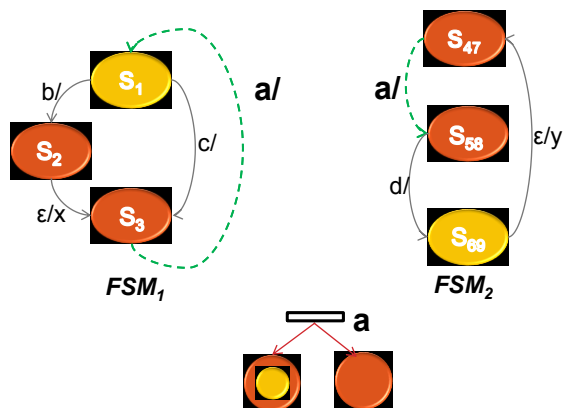
Synchronization Integration

► 25

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Synchronisation Primitive Extraction

► Step 3/4



PTNet to S-Component Decomposition

S-Component to FSM Mapping

Synchronization Primitive Extraction

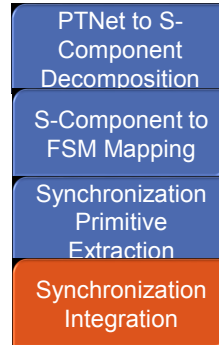
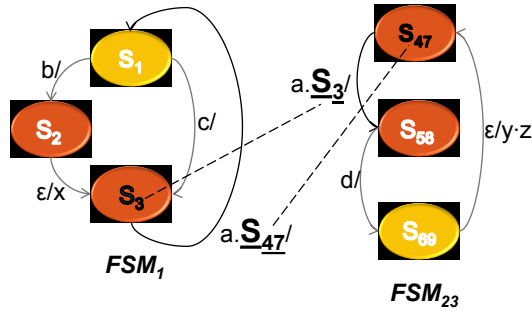
Synchronization Integration

► 26

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Synchronisation Integration

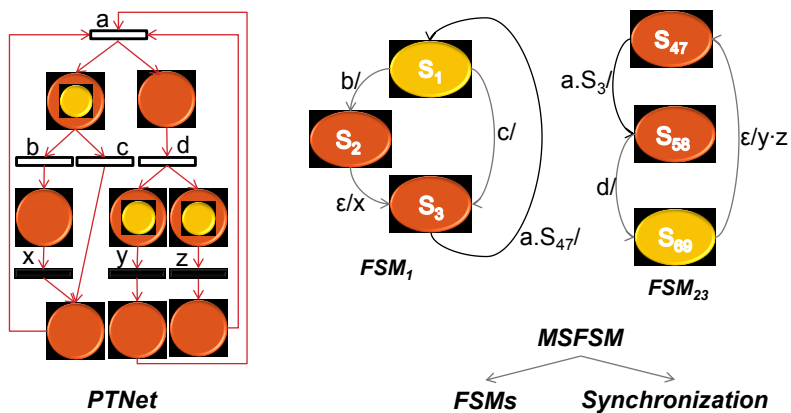
► Step 4/4



► 27

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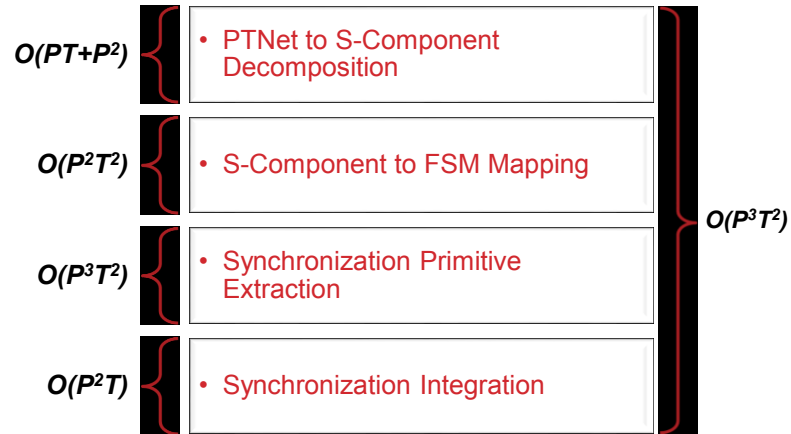
Resultant MSFSM Decomposition



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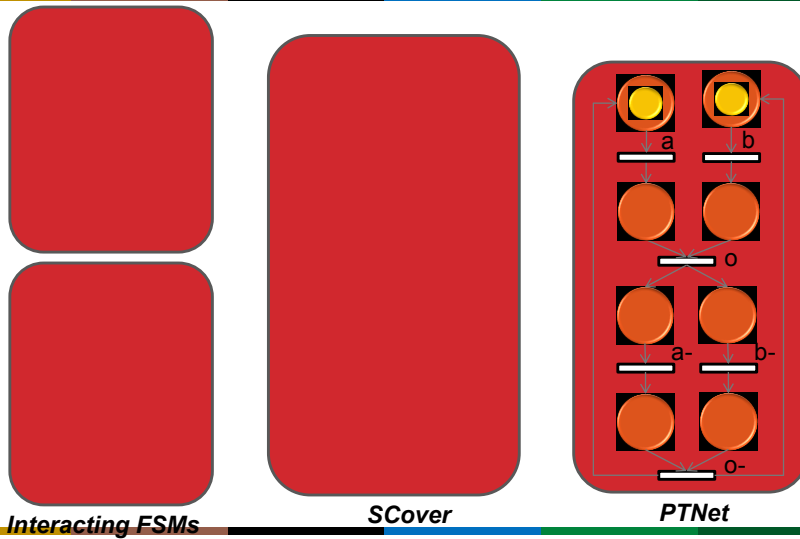
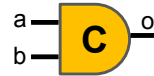
Complexity Analysis



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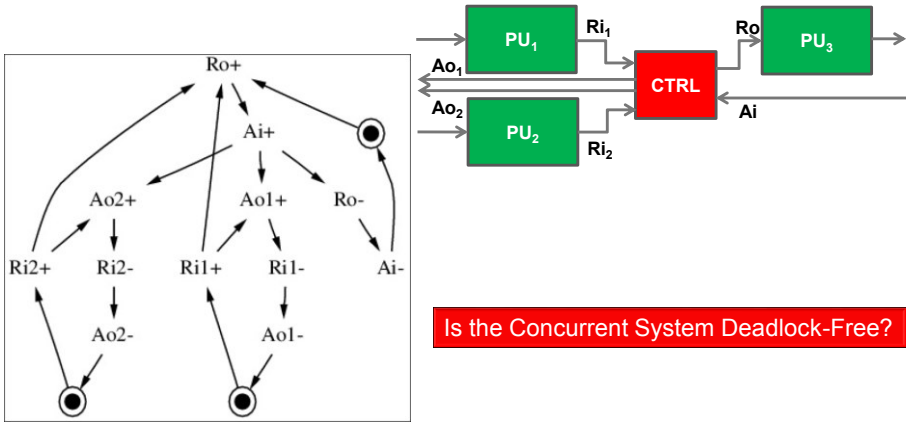
From MSFSMs to PTnets



▶ 30

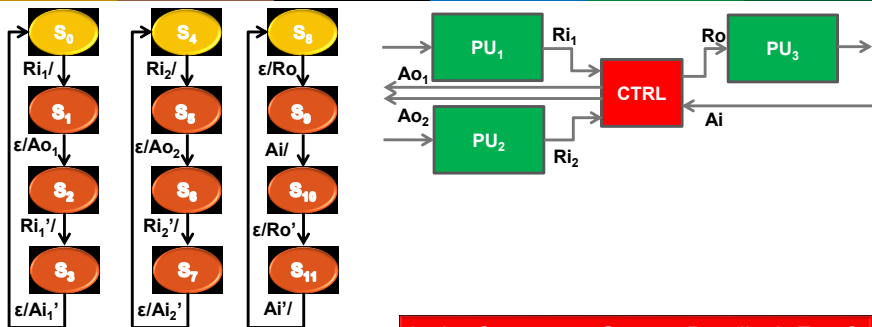
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MFSM-based Verification



Is the Concurrent System Deadlock-Free?

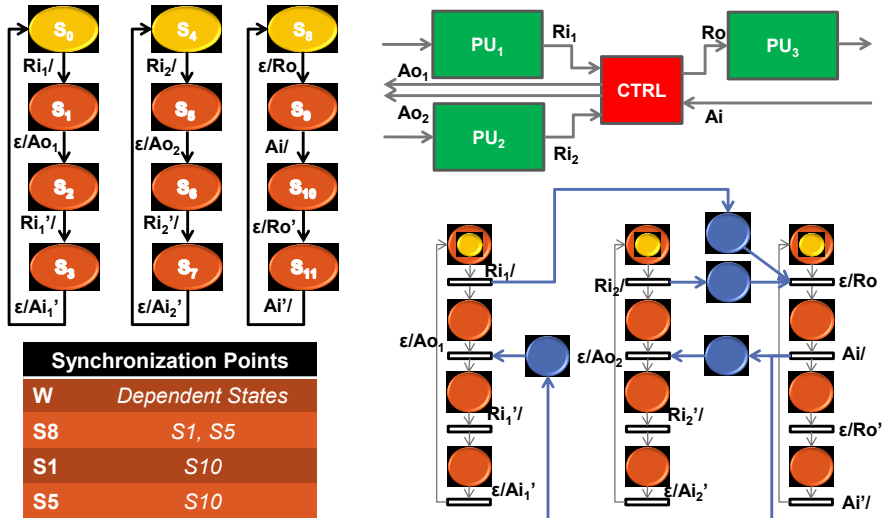
MFSM-based Verification



Is the Concurrent System Deadlock-Free?

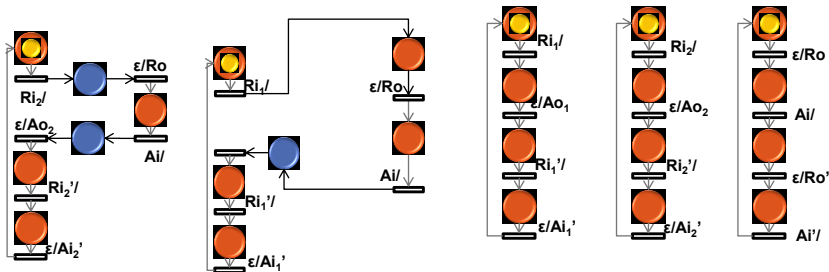
Synchronization Points	
W	Dependent States
S8	S1, S5
S1	S10
S5	S10

MFSM-based Verification



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MFSM-based Verification



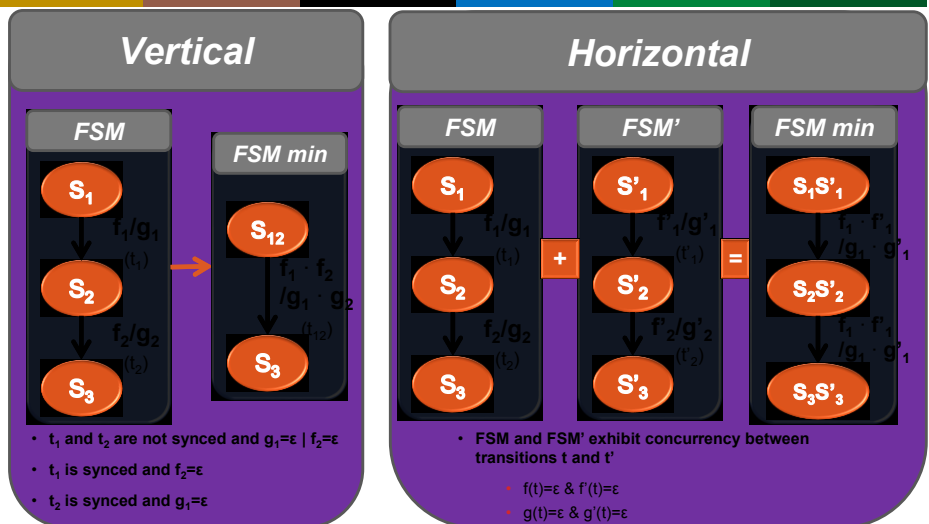
The system is covered by 5 initially marked minimal siphons.

Deadlock-Free

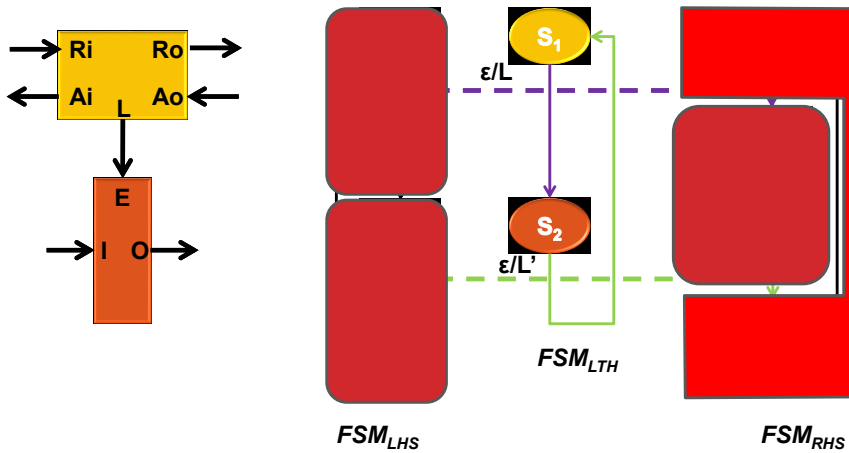
▶ 34

MSFSM Optimisations

Horizontal and Vertical State Collapsing, State Minimisation



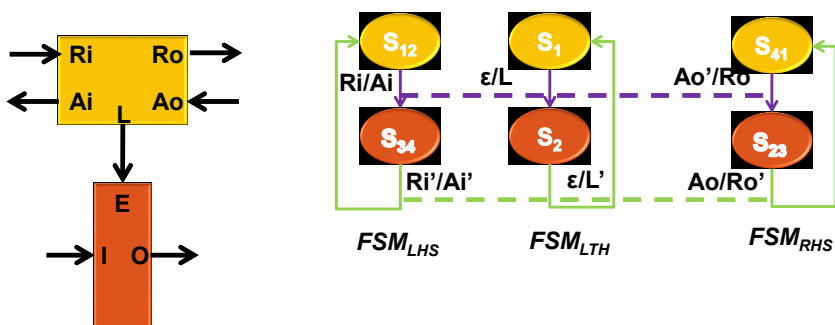
Horizontal and Vertical State Collapsing, State Minimisation



▶ 37

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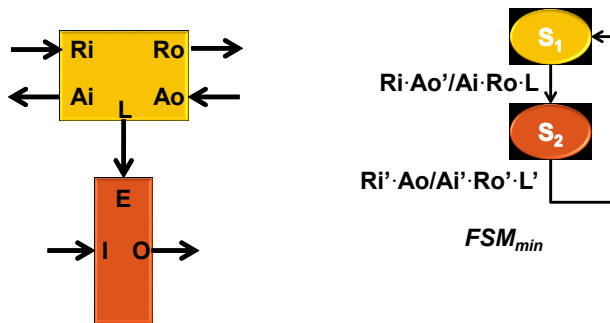
Horizontal and Vertical State Collapsing, State Minimisation



▶ 38

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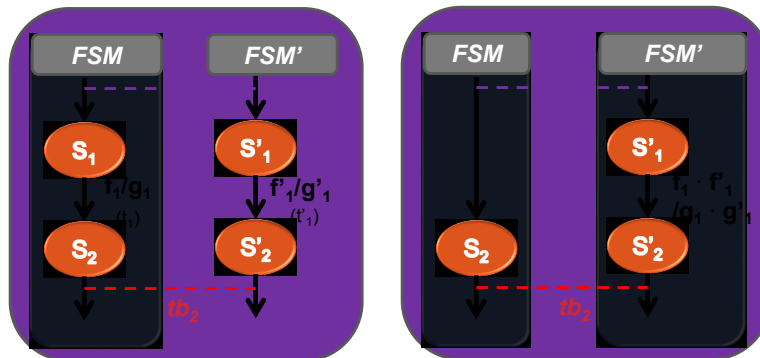
Horizontal and Vertical State Collapsing, State Minimisation



▶ 39

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The notion of MSFSM Cross(X)-Compatibles

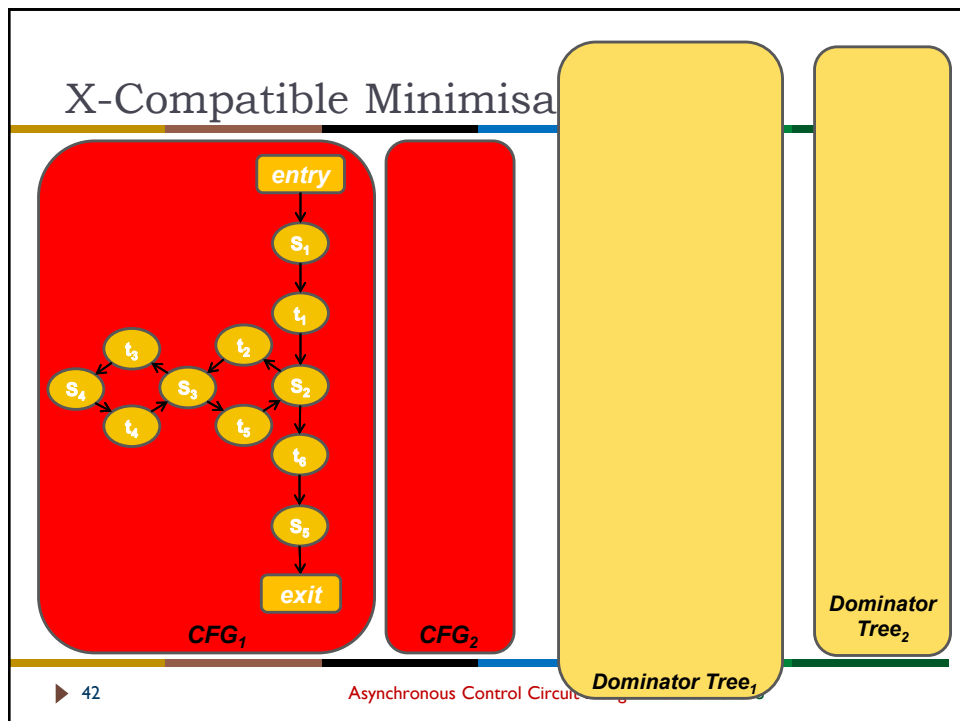
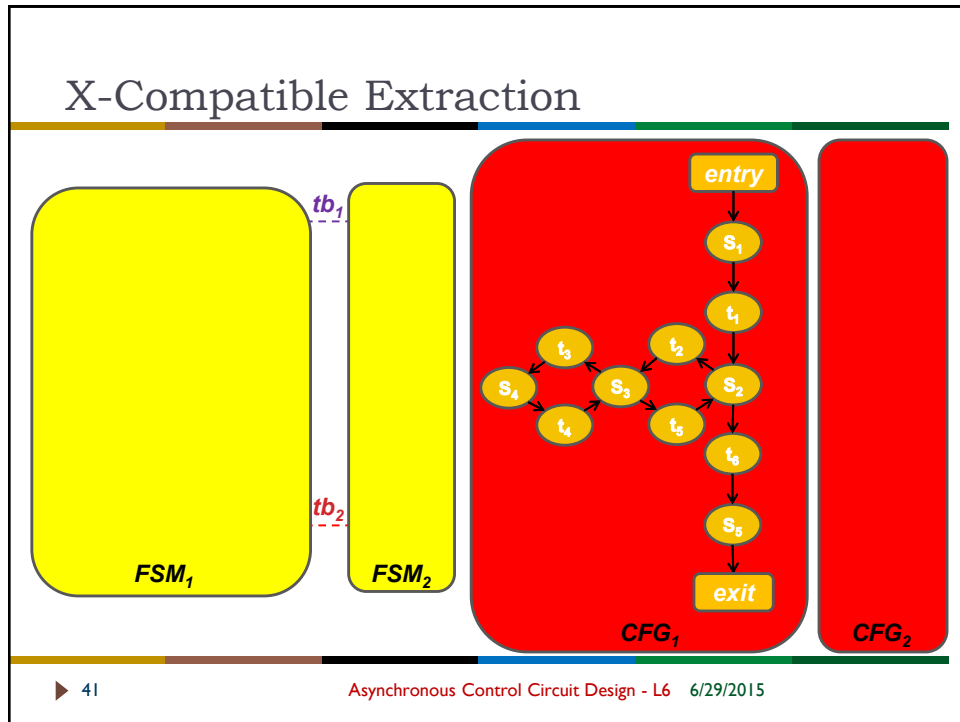


• Two transitions are X-Compatible if they are concurrent and mutually inclusive.

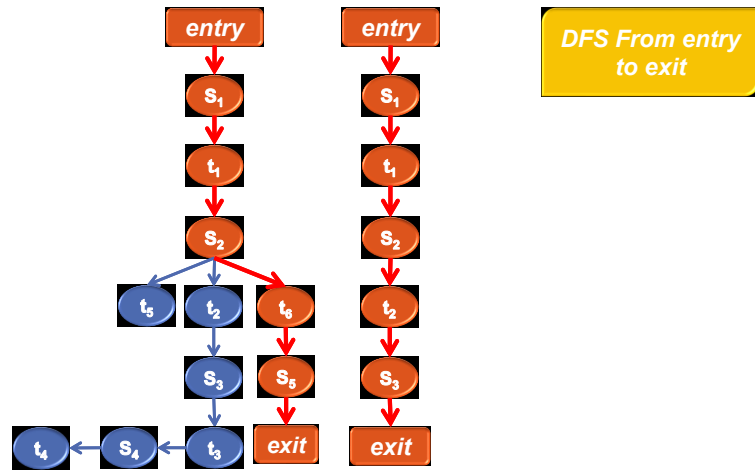
• t_1 and t'_1 are X-Compatible

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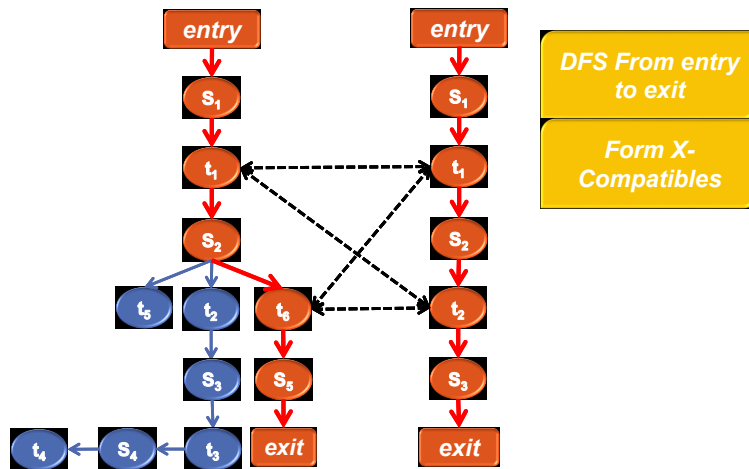
X-Compatible Minimisation



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X-Compatible Minimisation



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X-Compatible Minimisation

The diagram illustrates the X-Compatible Minimisation process for two FSMs, FSM_1 and FSM_2 . FSM_1 is represented by a large yellow rounded rectangle, and FSM_2 is a smaller yellow rounded rectangle. The process involves identifying common states between the two FSMs. This is shown by two horizontal dashed green lines, labeled tb_{cc1} and tb_{cc2} , which represent common states. Above FSM_1 , a dashed purple line is labeled tb_1 , and below FSM_2 , a dashed red line is labeled tb_2 . To the right of the FSMs, a vertical stack of three yellow boxes contains the following steps: "DFS From entry to exit", "Form X-Compatibles", and "Synchronize".

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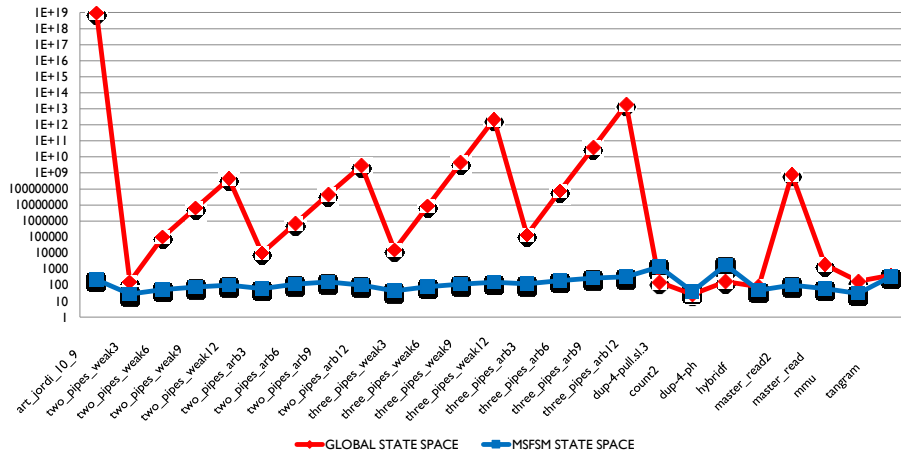
X-Compatible Minimisation

The diagram illustrates the X-Compatible Minimisation process for two FSMs, FSM_1 and FSM_2 . FSM_1 is represented by a large yellow rounded rectangle, and FSM_2 is a smaller yellow rounded rectangle. In this step, a specific state S_3 is identified in FSM_2 , highlighted by a black circle with a red border. A vertical arrow points from the top of FSM_2 down to S_3 . Above FSM_1 , a dashed purple line is labeled tb_1 , and below FSM_2 , a dashed red line is labeled tb_2 . To the right of the FSMs, a vertical stack of four yellow boxes contains the following steps: "DFS From entry to exit", "Form X-Compatibles", "Synchronize", and "Minimize".

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Results

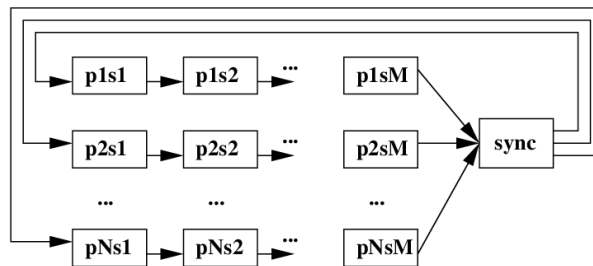
Global State Space vs. MSFSM State Space



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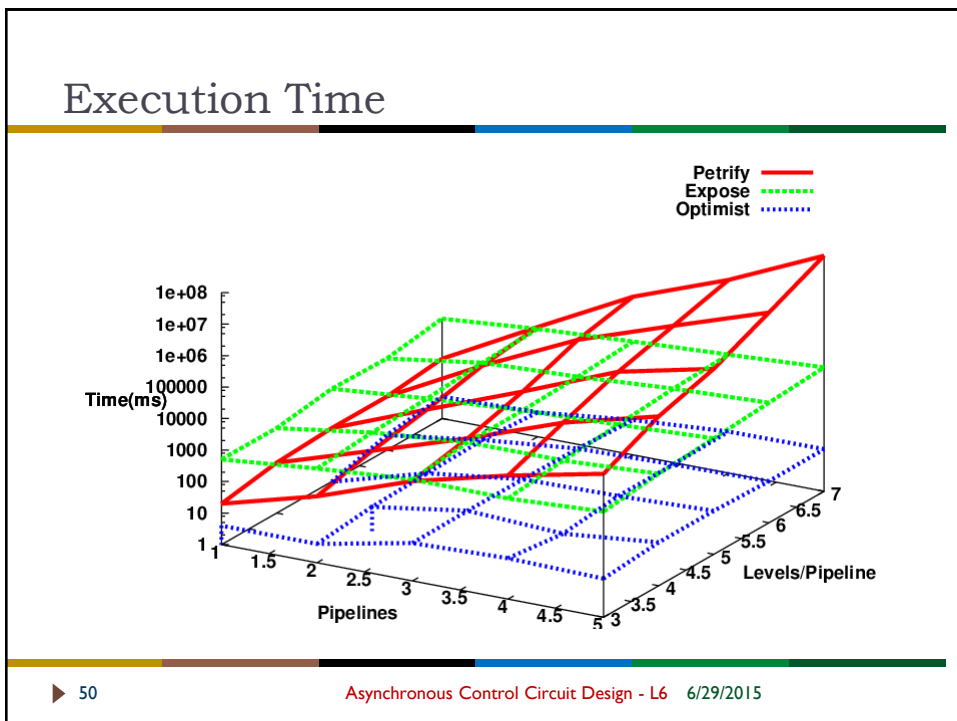
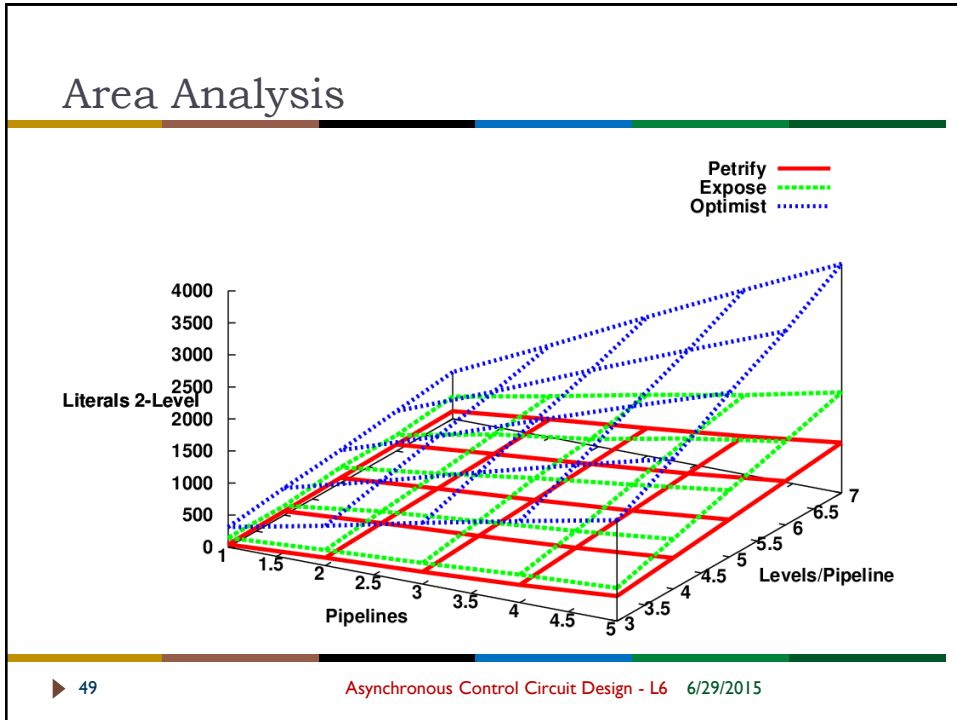
Asynchronous Synthesis Synthetic Benchmark



- ▶ N Parallel Handshake Controllers
- ▶ M Sequential Controllers Per Pipeline
- ▶ Synchronized at the M stage
 - ▶ Sync+ phase is a join, but Sync- is free (“loosely” synchronised)

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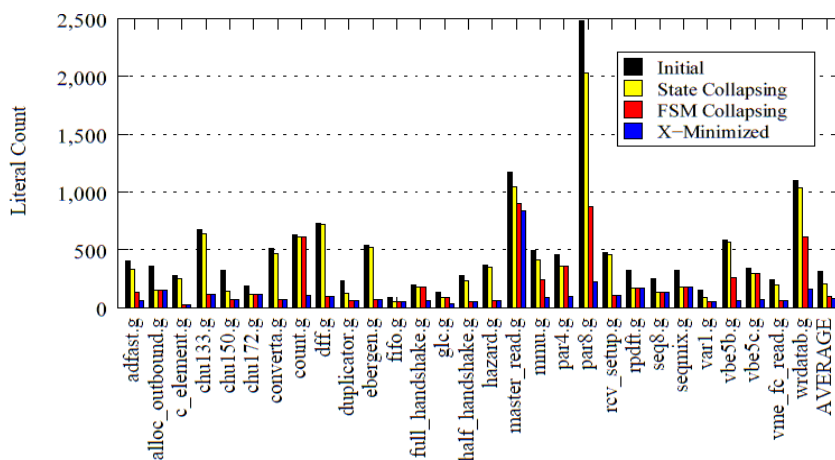
Asynchronous Control Circuit Area

Benchmark	Petrify	Optimist	Expose
alloc-outbound	66	258	30
c3	12	198	13
count2	<i>Irresolvable CSC</i>	302	178
dff	44	304	20
duplicator	93	228	111
full	44	264	102
half	43	198	148
monkey	<i>N/A</i>	1148	181
rpdf	34	214	25
semi-decoupled	86	242	208
vbe6a	132	732	237

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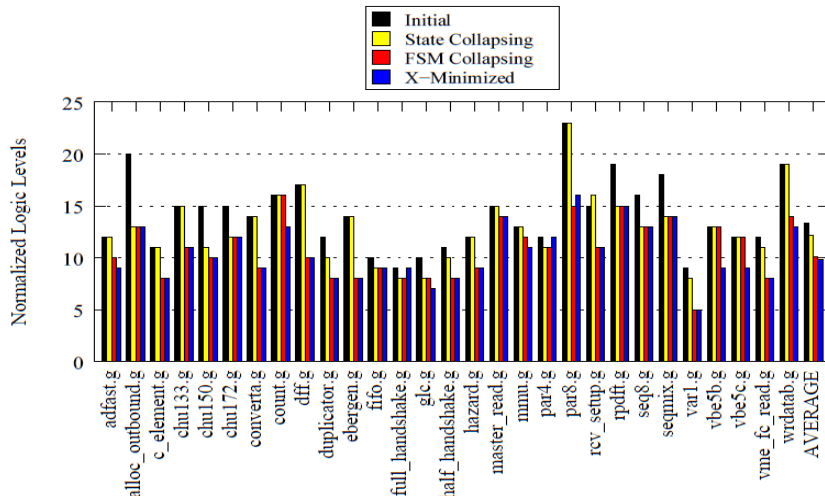
Optimisation – Literal Count (LC)



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Optimisation – Logic Depth



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Future Work

- ▶ Logic Synthesis of Mixed Synchronous and Asynchronous Circuits
 - ▶ Unified flow for Concurrent Control
- ▶ Examine Concurrency / Area Trade-Off possible by X-Compatible State/Segment Optimization
- ▶ Support more Asynchronous Timing Models
 - ▶ Speed Independent (SI)
 - ▶ State Encoding Requirements (Race-Free, Hazard-Free)

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