Monday 18
- 08:30 AM-09:00 AM Registration
- 09:00 AM-10:30 AM Hands-on Tutorial 1
  - HIFSuite for Cyber-physical VPs generation
    - Michele Lora, Univ. of Verona / EDALab
- 10:30 AM-11:00 AM Coffee break
- 11:00 AM-12:30 PM Hands-on Tutorial 2
  - The SPARK 2014 programming language
    - Martin Becker, Technical Univ. of Munich
- 12:30 PM-01:30 PM Lunch
- 01:30 PM-02:00 PM Opening remarks
  - Franco Fummi, Univ. of Verona
  - Hiren Patel, Univ. of Waterloo
  - Graziano Pravadelli, Univ. of Verona
- 02:00 PM-03:00 PM Keynote 1
  - IoT trends and innovative applications
    - Roberto Zafalon, STMicroelectronics
- 03:00 PM-03:30 PM Coffee break
- 03:30 PM-05:00 PM Session 1
  - Modeling and Simulation
    - Chair: Julio Medina, Univ. of Cantabria
      - 1. Fault Analysis in Linear Analog Circuits through Language Manipulation and Abstraction
        - Enrico Faccaroli, Univ. of Verona - Francesco Stefani, EDALab - Franco Fummi, Univ. of Verona - Mark Zvolinsky, Univ. of Southampton
      - 2. Actor Fission Transformations for Executing Dataflow Programs on Manycores
        - Essays Gebrewahid, Halmstad Univ. - Zain Ul-Abdin, Halmstad Univ.
      - 3. Rethinking of I/O-Automata Composition
        - Sarah Chabane, Univ. M Hamed Bougara - Rabea Zafalon Bougara, Université Paris-Saclay - Mohamed Mezhiche, Univ. M Hamed Bougara
- 05:00 PM-06:00 PM Panel 1
  - The WHAT and WHY? of high-level languages in designing and verifying complex integrated systems
    - Moderator: Sara Bocchio, STMicroelectronics
    - Nigel Woolaway, Leading Edge
    - Daniel Große, Univ. of Bremen
    - Massimo Roselli, Cadence Design Systems
- 06:00 PM-07:00 PM Welcome reception
- 07:00 PM-08:00 PM Welcome reception
- 08:00 PM-09:00 PM Welcome reception
- 09:00 PM-10:00 PM Welcome reception
- 10:00 PM-11:00 PM Welcome reception

Tuesday 19
- 08:30 AM-09:30 AM Keynote 2
  - Programming in a Heterogeneous World
    - Jan Kuper, QBayLogic
- 09:30 AM-11:00 AM Session 2
  - Languages and Design Methods for Time-critical Systems
    - Chair: Daniel Große, Univ. of Bremen
    - 2.1 Real-Time Ticks for Synchronous Programming
      - Reinhard von Hanxleden, Kiel Univ. - Timothy Bourke, INRIA, PARKAS Team - Alan Girault, INRIA, SPADES Team
    - 2.2 Symbolic Simulation of Dataflow Synchronous Programs with Timers
      - Guillaume Baudart, IBM Research - Timothy Bourke, INRIA/ENS - Marc Pouzet, LIENS
    - 2.3 Compositional Timing-Aware Semantics for Synchronous Programming
      - Joaquin Aguado, Univ. of Bamberg - Michael Mendler, Univ. of Bamberg - Ja Jo Wang, Univ. of Auckland - Bruno Bodini, Univ. of Edinburgh - Partha Koop, Univ. of Auckland
- 11:00 AM-11:30 AM Lunch
- 11:30 AM-01:00 PM Session 3
  - Programming Languages for Quantum Computing
    - Chair: Mathias Soeken, EPFL
    - 3.1 Benoit Valiron, CentraleSupelec, Univ. Paris-Saclay
    - 3.2 Nader Khammassi, TU Delft
    - 3.3 Michael Kirkedal Thomsen, Univ. of Copenhagen
- 01:00 PM-02:00 PM Lunch
- 02:00 PM-03:00 PM Panel 2
  - Languages for CPS: Are they needed?
    - Moderator: Nicola Bomberi, Univ. of verona
    - Julio Medina, Univ. de Cantabria
    - Sandeep Shukla, IIT Kanpur
    - Reinhard von Hanxleden, Kiel Univ.
- 03:00 PM-04:00 PM WIP Session + Posters
  - Chair: Daniel Große, Univ. of Bremen
  - WIP1 Error Propagation for Cascading Metamodels Applied on an Electric Drive Application
    - Christine Förster, Infineon - Manuel Harrant, Infineon - Jerome Kirscher, Infineon - Linus Maurer, Univ. der Bundeswehr München - Georg Pelz, Infineon
  - WIP2 From SQL to Database Processors: A Retargetable Query Planner?
    - Arda Yurdakul, Bogazici Univ.
  - WIP3 Towards MARTE++: An Enhanced UML-based Language to Model and Analyse Real-Time and Embedded Systems for the IoT Age
    - Julio L. Medina, Univ. de Cantabria - Eugenio Villar, Univ. de Cantabria
  - WIP4 Scalar Replacement with Array Dataflow Analysis for Hardware Synthesis
    - Kenshu Seto, Tokyo City Univ.
- 04:00 PM-04:30 PM Coffee break
- 04:30 PM-06:00 PM Session 4
  - Design and Validation Methodologies
    - Chair: Tom Kazmierski, Univ. of Southampton
    - 4.1 Automatic Generation of Cycle-Accurate Simulink Blocks from HDL IPs
      - Stefano Centomo, Univ. of Verona - Michele Lora, Univ. of Verona - Antonio Portaroli, EDALab - Francesco Stefani, EDALab - Franco Fummi, Univ. of Verona
    - 4.2 Towards Consistency Checking Between HDL and UPF Descriptions
      - Arthur Kaisling, TIMA Laboratory - Laurent Fesquet, TIMA Laboratory - Chouki Akouf, Defacto Technologies
    - 4.3 Towards Early Validation of Firmware-Based Power Management Using Virtual Prototypes: A Constrained Random Approach
      - Vladimir Herdt, Univ. of Bremen - Hoang M. Le, Univ. of Bremen - Daniel Große, Univ. of Bremen & DFKI - Rolf Drechsler, Univ. of Bremen & DFKI
- 06:00 PM-10:00 PM Social Event

Wednesday 20
- 08:30 AM-09:30 AM Keynote 3
  - Do Design/Specification Languages have any role to play in Cyber-Security?
    - Sandeep Shukla, IIT Kanpur
- 09:30 AM-11:00 AM Session 5
  - Next generation many-cores
    - Chair: Nicola Bomberi, Univ. of Verona
    - 5.1 Language and Hardware Acceleration Backend for Graph Processing
      - Andrey Mokhov, Newcastle Univ. - Alessandro de Gennaro, Newcastle Univ. - Gaith Taranewn, Newcastle Univ. - Jonny Wray, e-Therapeutics - Georg Lukyanov, Newcastle Univ. - Sergey Mileiko, Newcastle Univ. - Joe Scott, Newcastle Univ. - Alex Yakoiev, Univ. of Newcastle - Andrew Brown, Univ. of Southampton
    - 5.2 Runtime Task Mapping for Lifetime Budgeting in Many-Core Systems
      - Liang Wang, The Chinese Univ. of Hong Kong - Khaoshang Wang, South China Univ. of Technology - Ho-fung Leung, The Chinese Univ. of Hong Kong - Terence Mak, Univ. of Southampton
    - 5.3 A Reconfigurable Bit-serial FFT/FIR Processor for Ultra-low-power Applications
      - Yue Lu, Univ. of Southampton - Tom Kazmierski, Univ. of Southampton
- 11:00 AM-11:30 AM Coffee break
- 11:30 AM-01:00 PM Session 6
  - Design, Optimization, and Verification of Modern Industry Applications
    - Chair: Ashraf Salem, Mentor Graphics
    - 6.1 Identifying Bottlenecks in Manufacturing Systems Using Stochastic Criticality Analysis
      - João Bastos, Eindhoven Univ. of Technology - Bram van der Sanden, Eindhoven Univ. of Technology - Olaf Donk, ICT Group - Jeroen Voeten, Eindhoven Univ. of Technology - Sander Stuijk, Eindhoven Univ. of Technology - Ramon Schifferers, Eindhoven Univ. of Technology - Henk Corporaal, Eindhoven Univ. of Technology
    - 6.2 ASIL Decomposition Using SMF
      - Mona Safar, Ain Shams Univ.
    - 6.3 Multi-Objective Optimization-based Development of Power Electronics for Automotive Applications
      - Jonas Stricker, Universität der Bundeswehr München - Benno Köppl, Infineon Technologies - Ingrid Kirsch, Infineon Technologies - Thomas Nirmair, Infineon Technologies - Linus Maurer, Universität der Bundeswehr München - Georg Pelz, Infineon Technologies
    - 6.4 An Emulation Framework for Closed Source Components on a Multi-core Automotive Platforms
      - Ignacio Saffudo, Univ. of Modena and Reggio Emilia - Paolo Burigo, Univ. of Modena and Reggio Emilia - Marco Bertogna, University of Modena
- 01:30 PM-3:00 PM Lunch and closing